1) Who is the brain of computer:

a. ALU

b. CPU

c. MU

d. None of these

2) Which technology using the microprocessor is fabricated on a single chip:

a. POS

b. MOS

c. ALU

d. ABM

3) MOS stands for:

a. Metal oxide semiconductor

b. Memory oxide semiconductor

c. Metal oxide select

d. None of these

4) In which form CPU provide output:

a. Computer signals

b. Digital signals

c. Metal signals

d. None of these

5) How many types of microprocessor comprises:

a. 3

b. 6

c. 9

d. 4

6) Which is the microprocessor comprises:

a. Register section

b. One or more ALU

c. Control unit

d. All of these

7) The register section is related to_____ of the computer:

a. Processing

b. ALU

c. Main memory

d. None of these

8) What is the store by register:

a. data

b. operands

c. memory

d. None of these

9) How many types of classification of processor based on register section:

a. 1

b. 2

c. 3

d. 4

10) In Microprocessor one of the operands holds a special register called:

a. Calculator

b. Dedicated

c. Accumulator

d. None of these

11) Accumulator based microprocessor example are:

a. Intel 8085

b. Motorola 6809

c. A and B

d. None of these

12) A set of register which contain are:

a. data

b. memory addresses

c. result

d. all of these

13) How many types are primarily register:

a. 1

b. 2

c. 3

d. 4

14) There are primarily two types of register:

a. general purpose register

b. dedicated register

c. A and B

d. none of these

15) Which register is a temporary storage location:

a. general purpose register

b. dedicated register

c. A and B

d. none of these

16) How many parts of dedicated register:

a. 2

b. 4

c. 5

d. 6

17) Name of typical dedicated register is:

a. PC

b. IR

c. SP

d. All of these

18) PC stands for:

a. Program counter

b. Points counter

c. Paragraph counter

d. Paint counter

19) IR stands for:

a. Intel register

b. In counter register

c. Index register

d. Instruction register

20) SP stands for:

a. Status pointer

b. Stack pointer

c. a and b

d. None of these

21) The act of acquiring an instruction is referred as the____ the instruction:

a. Fetching

b. Fetch cycle

c. Both a and b

d. None of these

22) How many bit of instruction on our simple computer consist of one____:

a. 2-bit

b. 6-bit

c. 12-bit

d. None of these

23) How many parts of single address computer instruction :

a. 1

b. 2

c. 3

d. 4

24) Single address computer instruction has two parts:

a. The operation code
b. The operand
c. A and B
d. None of these

25) LA stands for:
a. Load accumulator
b. Least accumulator
c. Last accumulator
d. None of these

26) ED stands for:
a. Enable MRD
b. Enable MDR
c. Both a and b
d. None of these

27) LM stands for:
a. Least MAR
b. Load MAR
c. Least MRA
d. Load MRA

28) Causing a flag to became 0 is called:
a. Clearing a flag
b. Case a flag
c. Both a and b
d. None of these

29) Which are the flags of status register:
a. Over flow flag
b. Carry flag
c. Half carry flag
d. Zero flag
e. Interrupt flag
f. Negative flag
g. All of these

30) The carry is operand by:
a. C

31) The sign is operand by:
a. S

32) The zero is operand by:
a. Z

33) The overflow is operand by:

a. O

34) _____ is the condition:

a. CD

b. IR

c. Both a and b

d. None of these

35) ____ causes the address of the next microprocessor to be obtained from the memory:

a. CRJA

b. ROM

c. MAP

d. HLT

36) _____ Stores the instruction currently being executed:

a. Instruction register

b. Current register

c. Both a and b

d. None of these

37) In which register instruction is decoded prepared and ultimately executed:

a. Instruction register

b. Current register

c. Both a and b

d. None of these

38) The status register is also called the____:

a. Condition code register

b. Flag register

c. A and B

d. None of these

39) BCD stands for:

a. Binary coded decimal

b. Binary coded decoded

c. Both a & b

d. none of these

40) Which is used to store critical pieces of data during subroutines and interrupts:

a. Stack

b. Queue

c. Accumulator

d. Data register

41) The area of memory with addresses near zero are called:

a. High memory

b. Mid memory

c. Memory

d. Low memory

42) The point where control returns after a subprogram is completed is known as the :

a. Return address

b. Main Address

c. Program Address

d. Current Address

43) The subprogram finish the return instruction recovers the return address from the:

a. Queue

b. Stack

c. Program counter

d. Pointer

44) The processor uses the stack to keep track of where the items are stored on it this by using the:

a. Stack pointer register

b. Queue pointer register

c. Both a & b

d. None of these

45) Which point to the ___ of the stack:

a. TOP

b. START

c. MID

d. None of these

46) Stack words on:

a. LILO

b. LIFO

c. FIFO

d. None of these

47) Which is the basic stack operation:

a. PUSH

b. POP

c. BOTH A and B

d. None of these

48) SP stand for:

a. Stack pointer

b. Stack pop

c. Stack push

d. None of these

49) How many bit stored by status register:

a. 1 bit

b. 4 bit

c. 6 bit

d. 8 bit

50) Which is the important part of a combinational logic block:

a. Index register

b. Barrel shifter

c. Both a & b

d. None of these

51) The structure of the stack is _____ type structure:

a. First in last out

b. Last in last out

c. Both a & b

d. None of these

52) The data in the stack is called:

a. Pushing data

b. Pushed

c. Pulling

d. None of these

53) The CU is designed by using which techniques:

a. HARDWIRED CONTROLS

b. MICROPROGRAMING

c. NANOPROGRAMING

d. ALL OF THESE

54) The 16 bit register is separated into groups of 4 bit where each groups is called:

a. BCD

b. Nibble

c. Half byte

d. None of these

55) A nibble can be represented in the from of:

a. Octal digit

b. Decimal

c. Hexadecimal

d. None of these

56) The left side of any binary number is called:

a. Least significant digit

b. Most significant digit

c. Medium significant digit

d. low significant digit

57) MSD stands for:

a. Least significant digit

b. Most significant digit

c. Medium significant digit

d. low significant digit

58) _____ a subsystem that transfer data between computer components inside a computer or between computer:

a. Chip

b. Register

c. Processor

d. Bus

59) Which is called superhighway:

a. Processor

b. Multiplexer

c. Backbone bus

d. None of these

60) The external system bus architecture is created using from _____ architecture:

a. Pascal

b. Dennis Ritchie

c. Charles Babbage

d. Von Neumann

61) The network of wires or electronic path ways on mother board back side:

a. PCB

b. BUS

c. BOTH A and B

d. None of these

62) Which Bus connects CPU & level 2 cache:

a. Rear side bus

b. Front side bus

c. Memory side bus

d. None of these

63) Which bus carry addresses:

a. System bus

b. Address bus

c. Control bus

d. Data bus

64) A 16 bit address bus can generate___ addresses:

a. 32767

b. 25652

c. 65536

d. none of these

65) The processor 80386/80486 and the Pentium processor uses _____ bits address bus:

a. 16

b. 32

c. 36

d. 64

66) CPU can read & write data by using :

a. Control bus

b. Data bus

c. Address bus

d. None of these

67) Which bus transfer singles from the CPU to external device and others that carry singles from external device to the CPU:

a. Control bus

b. Data bus

c. Address bus

d. None of these

68) Which is not the control bus signal:

a. READ

b. WRITE

c. RESET

d. None of these

69) When memory read or I/O read are active data is to the processor :

a. Input

b. Output

c. Processor

d. None of these

70) When memory write or I/O read are active data is from the processor:

a. Input

b. Output

c. Processor

d. None of these

71) Using 12 binary digits how many unique house addresses would be possible:

a. 2^8=256

b. 2^{12}=4096

c. 2^{16}=65536

d. None of these

72) PROM stands for:

a. Programmable read-only memory

73) EPROM stands for:

a. Erasable Programmable read-only memory

74) Each memory location has:

a. Address

b. Contents

c. Both A and B

d. None of these

75) Which is the type of microcomputer memory:

a. Processor memory

b. Primary memory

c. Secondary memory

d. All of these

76) Secondary memory can store____:

a. Program store code

b. Compiler

c. Operating system

d. All of these

77) Secondary memory is also called____:

a. Auxiliary

b. Backup store

c. Both A and B

d. None of these

78) Customized ROMS are called:

a. Mask ROM

b. Flash ROM

c. EPROM

d. None of these

79) The ram which is created using bipolar transistors is called:

a. Dynamic RAM

b. Static RAM

c. Permanent RAM

d. DDR RAM

80) Which type of RAM needs regular referred:

a. Dynamic RAM

b. Static RAM

c. Permanent RAM

d. SD RAM

81) Which RAM is created using MOS transistors:

a. Dynamic RAM

b. Static RAM

c. Permanent RAM

d. SD RAM

82) Which latch is mostly used creating memory register:

a. SR-Latch

b. JK-Latch

c. D-Latch

d. T-Latch

83) Which statement is false about WR signal:

a. WR signal controls the input buffer

b. The bar over WR means that this is an active low signal

c. The bar over WR means that this is an active high signal

d. If WR is 0 then the input data reaches the latch input

84) Which technique is used for main memory array design:

a. Linear decoding

b. Fully decoding

c. Both A and B

d. None of these

85) CS stands for:

a. Cable select

b. Chip select

c. Control select

d. Cable system

86) WE stands for:

a. Write enable

b. Wrote enable

c. Write envy

d. None of these

87) When CS _____ the chip is not selected at all hence D7 to D0 are driven to high impedance state:

a. High

b. Low

c. Medium

d. Stand by

88) The capacity of this chip is 1KB they are organized in the form of 1024 words with 8 bit word The what is the site of address bus:

a. 8 bit

b. 10 bit

c. 12 bit

d. 16 bit

89) Which storage technique dose not decoding circuit:

a. Linear decoding

b. Fully decoding

c. Partially

d. None of these

90) In linear decoding address bus of 16-bit wide can connect only ____ of RAM.

a. 16 KB

b. 6KB

c. 12KB

d. 64KB

91) Which statement is wrong according to linear decoding :

a. Address map is not contiguous.

b. Confects occur if two of the select lines become active at the same time

c. If all unused address lines are not used as chip selectors then these unused lines become don't cares

d. None of these

92) The problem of bus confect and sparse address distribution are eliminated by the use of _____ address technique:

a. Fully decoding

b. Half decoding

c. Both a & b

d. None of these

93) A microprocessor retries instructions from :

a. Control memory

b. Cache memory

c. Main memory

d. Virtual memory

94) Which register is used to communicate with memory:

a. MAR

b. MDR

c. Both A and B

d. None of these

95) SAM stands for:

a. Simple architecture machine

b. Solved architecture machine

c. Both a & b

d. None of these

96) MAR stands for:

a. Memory address register

b. Memory address recode

c. Micro address register

d. None of these

97) MDR stands for:

a. Memory data register

b. Memory data recode

c. Micro data register

d. None of these

98) VAM stands for:

a. Valid memory address

b. Virtual memory address

c. Variable memory address

d. None of these

99) Which microprocessor to read an item from memory:

a. VAM

b. SAM

c. MOC

d. None of these

100) Which bus plays a crucial role in I/O:

a. System bus

b. Control bus

c. Address bus

d. Both A and B

101) Which register is connected to the memory by way of the address bus:

a. MAR

b. MDR

c. SAM

d. None of these

102) How many bit of MAR register:

a. 8-bit

b. 16-bit

c. 32-bit

d. 64-bit

103) MOC stands for:

a. Memory operation complex

b. Micro operation complex

c. Memory operation complete

d. None of these

104) Which are the READ operation can in simple steps:

a. Address

b. Data

c. Control

d. All of these

105) The upper red arrow show that CPU sends out the control signals____ and _____ indicate the data is read from the memory:

a. Memory request

b. Read

c. Both A and B

d. None of these

106) The information is transferred from the_____ and ____ specified register:

a. MDR

b. CPU

c. Both A and B

d. None of these

107) The information on the data bus is transferred to the _____register:

a. MOC

b. MDR

c. VAM

d. CPU

108) The lower red curvy arrow show that CPU places the address extracted from the memory location on the_____:

a. Address bus

b. System bus

c. Control bus

d. Data bus

109) DMA stands for:

a. Direct memory access

b. Direct memory allocation

c. Data memory access

d. Data memory allocation

110) DMA stands for:

a. Dynamic memory access

b. Data memory access

c. Direct memory access

d. Both B and C

111) CRT stands for:

a. Cathode ray tube
b. Compared ray tube
c. Command ray tube
d. None of these

112) The CPU sends out a ____ signal to indicate that valid data is available on the data bus:
a. Read
b. Write
c. Both A and B
d. None of these

113) The ____ place the data from a register onto the data bus:
a. CPU
b. ALU
c. Both A and B
d. None of these

114) The CPU removes the ___ signal to complete the memory write operation:
a. Read
b. Write
c. Both A and B
d. None of these

115) The value memvar must be transferred to the ___:
a. Computer
b. CPU
c. Both A and B
d. None of these

116) The microcomputer system by using the ____device interface:
a. Input
b. Output
c. Both A and B
d. None of these

117) How bit microprocessor inexpensive a separate interface is provided with I/O device:
a. 2 bit
b. 4 bit
c. 8 bit
d. 32 bit

118) How many ways of transferring data between the microprocessor and a physical I/O device:
a. 2
b. 3
c. 4

d. 5

119) The standard I/O is also called:

a. Isolated I/O

b. Parallel I/O

c. both a and b

d. none of these

120) standard I/O uses which control pin on the micro processor:

a. IO/M

121) A___ on this pin indicates a memory operation:

a. Low

b. High

c. Medium

d. None of these

122) The external device is connected to a pin called the _____ pin on the processor chip.

a. Interrupt

b. Transfer

c. Both

d. None of these

123) The DMA controllers are special hardware embedded into the chip in modern integrate processor that ____and_____ to the system;

a. Data transfer

b. arbitrate access

c. Both A and B

d. None of these

124) The CPU completes yields control of the bus to the DMA controller via:

a. DMA acknowledge signal

b. DMA integrated signal

c. DMA implicitly signal

d. None of these

125) The mode of DMA are:

a. Single transfer

b. Block transfer

c. Burst –block transfer

d. Repeated single transfer

e. Repeated–block transfer

f. Repeated Burst –block transfer

g. All of these

---

1. EOC stands for:

a. End of conversion
b. Emphasize of conversion
c. End of controller
d. None of these

2. IRR stands for:
a. Interrupt request register
b. Input request register
c. Interrupt resolver register
d. Input resolver register

3. ISR stands for:
a. Interrupt service register
b. Input service register
c. In-service register
d. All of these

4. PR stands for:
a. Priority register
b. Priority resolver
c. Priority request
d. None of these

5. IMR stands for:
a. Input mask register
b. Input mask resolver
c. Interrupt mask resolver
d. Interrupt mask register

6. INT stands for:
a. Input
b. Interrupt
c. Both a and b
d. None of these

7. INTA stands for:
a. Interrupt acknowledge
b. Interrupt access
c. Interrupt address
d. None of these

8. CS stands for:
a. Command select
b. Chip select
c. Chip series
d. Command series

9. RD stands for:
   - **a. Read**
   - b. Register
   - c. Request
   - d. Real

10. ICW stands for:
   - a. Interrupt command words
   - b. Interrupt command write
   - **c. Initialization command words**
   - d. Initialization command write

11. OCW stands for:
   - **a. Operational command words**
   - b. Operational conjunction words
   - c. Operational control words
   - d. Operational cost words

12. DMA stands for:
   - a. Direct memory allocation
   - **b. Direct memory access**
   - c. Direct memory application
   - d. Direct memory acknowledgment

13. HLD stands for:
   - a. High
   - b. Hour
   - **c. Hold**
   - d. None of these

14. HLDA stands for:
   - a. High acknowledgment
   - **b. Hold acknowledgment**
   - c. High access
   - d. Hold access

15. HRQ stands for:
   - **a. Hold request**
   - b. Hold read
   - c. Hold register
   - d. Hold resolver

16. AEN stands for:
   - **a. Address enable**
   - b. Address equivalent
   - c. Acknowledgment enable

d. Acknowledgment equivalent

17. ADSTB stands for:

a. Access strobe

b. Access strobe

c. Address store

d. Address strobe

18. MEMER and MEMW means:

a. Memory read

b. Memory write

c. Both a and b

d. None of these

19. HRQ and HLDA means:

a. Hold request

b. Hold acknowledgment

c. Both a and b

d. None of these

20. ADC stands for:

a. Analogue to analogue converters

b. Analogue to digital converters

c. Digital to digital converters

d. Digital to analogue converters

21. DAC stands for:

a. Analogue to analogue converters

b. Analogue to digital converters

c. Digital to digital converters

d. Digital to analogue converters

22. Which is the commonly used programmable interface and particular used to provide handshaking:

a. 8251

b. 8254

c. 8259

d. 8255

23. Which is a programmable communication interface:

a. 8255

b. 8254

c. 8251

d. 8259

24. Which programmable timer is used to generate timing signal :

a. 8255

b. 8254

c. 8251

d. 8259

25. Which is widely used in interrupt controller with a number of microprocessor:

a. 8251

b. 8254

c. 8255

d. 8259

26. Which are used DMA controllers with 8085/8086 microprocessor:

a. 8237

b. 8257

c. Both a and b

d. None of these

27. Which provide a mechanism to establish a link between the microprocessor and i/o device:

a. Input interface

b. Output interface

c. Both a and b

d. None of these

28. In which the processor uses a protection of the memory address to represent I/O ports:

a. Memory mapped I/O

b. I/O memory mapped

c. Both a and b

d. None of these

29. The standard I /O is also called:

a. I/O mapped I/O

b. Isolated I/O

c. Both a and b

d. None of these

30. The processor of knowing the status of device and transferring the data with matching speeds is called:

a. Handshaking

b. Peripheral

c. Ports

d. None of these

31. Which is designed to automatically manage the handshake operation:

a. 8251

b. 8254

c. 8255

d. 8259

32. Which mode is used for single handshake in 8255:

a. Mode 0

b. Mode 1

c. Mode 2

d. None of these

33. Which mode is used for double handshake in 8255:

a. Mode 0

b. Mode 1

c. Mode 2

d. None of these

34. Which mode is used for simple input or output without handshaking:

a. Mode 0

b. Mode 1

c. Mode 2

d. None of these

35. Which are used for port B in 8255:

a. PC0-PC2

b. PC3-PC7

c. PC6-PC7

d. PC3-PC5

36. Which are used for port A in 8255 mode 1:

a. PC0-PC2

b. PC3-PC7

c. PC6-PC7

d. PC3-PC5

37. Which are used for handshake lines for port A in 8255 mode 2:

a. PC0-PC2

b. PC3-PC7

c. PC6-PC7

d. PC3-PC5

38. AL&99H which operation is performed here:

a. Input

b. Output

c. Both a & b

d. None of these

39. 34H&AX which operation is performed here:

a. Input

b. Output

c. Progress

d. None of these

40. Which chip used for AD&DA converters in 8086 processor:

a. 8251

b. 8255

c. 8254

d. 8259

41. The time taken by the ADC from the active edge of SOC pulse till the active edge of EOC signal is called:

a. Conversion over

b. Conversion delay

c. Conversion signal

d. None of these

42. Arrange the flowing step of the general algorithm for ADC interfacing:

i. Issuing start of conversion pulse to ADC.

ii. Marking the end of the conversion processes by the.

iii. Read digital data output of the ADC as equivalent digital output.

iv. Ensuring the stability of analogue input applied to the ADC.

a. 2,1,3,4

b. 4,1,2,3

c. 1,2,3,4

d. 4,3,2,1

43. Which chip is used for analogue to digital converter:

a. 0809

b. 0808

c. Both a & b

d. None of these

44. Which multiplexer by ADC 0808/0809:

a. 2:4

b. 3:8

c. 4:16

d. None of these

45. Which chip is used for DAC:

a. AD7521

b. AD7522

c. AD7523

d. AD7524

46. Which converters convert binary number into their equivalent voltages:

a. Analogue to analogue

b. Analogue to digital

c. Digital to digital

d. Digital to analogue

47. An external feedback resistor acts to control the:

a. Gain

b. Gate

c. Loss

d. Profit

48. Which used to generate accurate time delays and can be used for other timing application such as a real time clock an event counter a digital one shot a square wave generator and a complex wave form generator:

a. 8251 programmable timer

b. 8255 programmable timer

c. 8254 programmable timer

d. 8259 programmable timer

49. 8254 programmable timer counter has two inputs signals:

a. CLK

b. Gate

c. Both a & b

d. None of these

50. 8254 programmable timer counter has:

a. 1output signal

b. 2output signal

c. 3output signal

d. 4output signal

51. 8254 can operate how many operating modes:

a. 2

b. 4

c. 6

d. 8

52. 8254 gate of a counter is to either:

a. Enable counting

b. Disable counting

c. Both

d. None of these

53. 8254 counters can count in the:

a. Binary
b. Decimal
c. Hexadecimal
d. A & B

54. How many modes in 8254:
a. 2
b. 4
c. 6
d. 8

55. Which is the state of gate signal for normal contains:
a. Low
b. High
c. Undefined
d. None of these

56. Which generate an interrupt to the microprocessor after a certain interval of time:
a. 8251
b. 8254
c. 8255
d. 8259

---

1. A central processing unit, fabricated on a single chip of semiconductor is called:

a. Microprocessor
b. RAM
c. ROM
d. None of these

2. Which is the architecture of microprocessor:

a. CISC
b. RISC
c. All of these
d. None of these

3. CISC stands for:
a. Complex Instruction System Computer
b. Complex Instruction Set Car

c. **Complex Instruction Set Computer**
d. None of these
4. RISC stands for:
a. Reduced Instruction Set Computer
b. Reduced Intergraded Set Computer
c. Resource Instruction Set Computer
d. Resource Instruction System Computer
5. Which is the components of computer:

a. System Bus
b. CPU
c. Memory Unit
d. All of these

6. System Bus Contains:

a. Address Bus
b. Data Bus
c. Control Bus
d. All of these

7. Microprocessor is the _____ of computer:

a. Hand
b. Heart
c. Brain
d. Leg

8. Microprocessor is fabricated on single chip using:

a. MOS
b. ALU
c. CPU
d. All of these

9. Which is the components of microprocessor:

a. Register unit
b. Arithmetic and logical unit

c. Timing and control unit
d. All of these

10. Which is an integral part of any microcomputer system and its primary purpose is to hold program and data:

a. Memory unit
b. Register unit
c. A and B
d. None of these

11. How many group of memory unit:

a. Four
b. Three
c. Two
d. One

12. Which is the parts of memory unit:

a. Processor memory
b. Main memory
c. Secondary memory
d. All of these

13. MOS stand for:

a. Metal oxide semiconductor
b. Memory oxide semiconductor
c. A and B
d. None of these

14. Which system communicates with the outside word via the I/O devices interfaced to it:

a. Microprocessor
b. Microcomputer
c. Digital computer
d. All of these

15. A computer which has the microprocessor as_____ is called as a microcomputer:

a. CPU
b. ALU
c. RU

d. None of these

16. The organization of I/O devices create a difference between _____:

a. Digital computer
b. Micro computer
c. A and B
d. None of these

17. How many generation of microprocessor:

a. Four
b. Five
c. Six
d. Three

18. The___ was very successful in the calculator market at that time:

a. Motorola 6800 and 6809
b. Microprocessor 4004
c. Intel 8085
d. None of these

19. How are the successful microprocessor:

a. 8004
b. 5006
c. 4004
d. All of these

20. How many microprocessor in the market during the same period:

a. 6

b. 8

c. 3

d. 5

21. PMOS stands for:

a. P-channel metal-oxide-semiconductor

b. P-channel memory –oxide-semiconductor

c. Both A and B

d. None of these

22. Which provided the current:

a. Low-cost

b. Slow-cost

c. Low-Output

d. All the above

23. Second Generation_____?

a. 1974-1976

b. 1974-1978

c. 1974-1972

d. None of these

24. The beginning of very efficient____ microprocessor in second generation:

a. 4-bit

b. 8-bit

c. 16-bit

d. 64-bit

25. Which are some of popular processor:

a. Motorola 6800 and 6809

b. Intel 8085

c. Zilog Z80

d. All the above

26. NMOS stands for:

a. N-channel metal-oxide-semiconductor

b. P-channel metal-oxide-semiconductor
c. N-channel memory-oxide-semiconductor
d. All the above

27. _____ Was more common year:

a. CRT
b. TTL
c. Both A and B
d. None of these

28. Which technology speed faster and higher density:

a. PMOS
b. NMOS
c. HMOS
d. All the above

29. What is the period of 3 generation:

a. 1979-1981
b. 1979-1980
c. 1978-1979
d. 1978-1980

30. Third generation microprocessor is dominated by____ microprocessor:

a. 8 bit
b. 4 bit
c. 16 bit
d. 64 bit

31. Intel used HMOS technology to recreate_____:

a. 8084 A
b. 8086 A
c. 8085 A
d. 8088 A

32. HMOS stands for:

a. High performance metal oxide semiconductor
b. High processor metal oxide semiconductor
c. Both A and b
d. None of these

33. What is the period of fourth generation:

a. 1979-1980
b. 1981-1995
c. 1995-2000
d. 1974-1980

34. The fourth generation of microprocessor came really as a soon boon to the_____:

a. Computing environment
b. Processing environment
c. Hot environment
d. All of these

35. How many bit microprocessor in the era marked beginning of fourth generation:

a. 4 bit
b. 8 bit
c. 16 bit
d. 32 bit

36. They were fabricated using a low power version of the HMOS technology called____:

a. HSMOS
b. HCMOS
c. HSSOM
d. None of these

37. Motorola introduced _____ processor:

a. 2 bit-RISC
b. 4 bit-RISC
c. 8 bit-RISC
d. 32 bit-RISC

38. Motorola introduced 32 bit RISC processor called_____:

a. MC 88100
b. MC 81100
c. MC 80100
d. MC 81000

39. Period of fifth generation?

a. 1974-1978
b. 1979-1980
c. 1981-1985
d. 1995-till date

40. The growth of vacuum tube technology has been listed as follow:

a. 1946-1957
b. 1958-1964
c. 1985-1999
d. None of these

41. The growth of transistor technology in_____:

a. 1946-1957
b. 1958-1964
c. 1985-1999
d. None of these

42. How are the growth of SSI technology in_____:

a. 1956 on words
b. 1965 on words
c. 1978 on words
d. 1978 on words

43. The growth of medium scale integration in_____:

a. Till 1971
b. Till 1970

c. Till 1972
d. Till 1969

44. The growth of SSI up to____:

a. 100 device on a chip
b. 200 device on a chip
c. 300 device on a chip
d. 400 device on a chip

45. The growth of LSI technology on_____:

a. 1994-1995
b. 1971-1977
c. 1972-1978
d. None of these

46. Which is most commonly measured in terms of MIPS previously million instruction per second:

a. Microprocessor
b. Performance of a microprocessor
c. Assembly line
d. None of these

47. The range of this rating for which microprocessor of_____:

a. VLSI
b. Motorola
c. Intel
d. Zilog

48. How can we make computers work faster?

a. The fetch-execute cycle and pipelining
b. The assembly
c. Both A and B
d. None of these

49. Who is the represents the fundamental process in the operation of the CPU:

a. The fetch-execute cycle and pipelining
b. The assembly
c. Both A and B

d. None of these

50. Which process information at a much faster rate than it can retrieve it from memory:

a. ALU
b. Processor
c. Microprocessor
d. CPU

51. _____ memory system which is discussed later can improve matters in this respect:

a. Data memory
b. Cache memory
c. Memory
d. None of these

52. The fetch-execute cycle is to use a system know as:

a. Assembly line
b. Pipelining
c. Cache
d. None of these

53. The time taken for all stages of the assembly line to become active is called the:

a. Flow through time
b. Clock period
c. Throughput
d. All of these

54. The clock period is denoted by:

a. T_p

b. $T_1+T_2+T_3--------+T_n$

c. P_t

d. None of these

55. T_i is the time taken for the ith stage and there are n stages in the:

a. Throughput

b. Assembly line

c. Both A and B

d. None of these

56. Who is the determined by the time taken by the stages the requires the most processing time:

a. Clock period

b. Flow through

c. Throughput

d. None of these

57. The _____ of can assembly line to be I/t_p:

a. Clock period

b. Pipelining

c. Throughput

d. Flow through

58. Which is the microprocessor launched by Motorola corporation introduced:

a. Mc6800

b. 8080

c. IMP-8

d. RPS-8

59. How many bit MC6800 microprocessor:

a. 4-bit

b. 8-bit

c. 16-bit

d. 32-bit

60. Motorola has declined from having nearly _____ share of the microprocessor market to much smaller share:

a. 30%
b. 40%
c. 50%
d. 60%

61. Which is the microprocessor launch by Fairchild company:

a. F-6
b. F-8
c. Both A and B
d. None of these

62. How many stages has fetch execute cycle:

a. 3
b. 4
c. 5
d. 6

63. Which is the world's first microprocessor?

a. Intel 4004
b. Motorola 68020
c. Intel8008
d. None of these

64. MOSFET stands for?
a. **Metal-oxide-semiconductor field effect transistor**
b. Metal-oxide-semiconductor fan effort transistor
c. Both A and B
d. None of these
65. What is the main problem of Intel 4004 microprocessor:

a. Speed
b. Memory size

c. World width
d. All of these

66. The evolution of the 4 bit microprocessor ended when Intel released in:

a. 4004
b. 8008
c. 40964
d. 4040

67. How many bit microprocessor still survives in low-end application such as microwave ovens and small control system:

a. 4 bit
b. 16 bit
c. 32 bit
d. 64 bit

68. Calculator are based on_____ microprocessor:

a. 4 bit
b. 16 bit
c. 32 bit
d. 64 bit

69. BCD stands for:

a. Binary coded decimal
b. Based coded decimal
c. Both A and B
d. None of these

70. Intel 8008 microprocessor realizing in:

a. 1971
b. 1973
c. 1999
d. 1988

71. Intel 8008 microprocessor's upgraded version is:

a. 8080
b. 4004
c. Both A and B
d. None of these

72. Intel 8008 microprocessor was introduced in:

a. 1971
b. 1973
c. 1999
d. 1988

73. MC6800 microprocessor was introduced by:

a. Motorola corporation
b. Fairchild
c. Both A and B
d. None of these

74. Which Microprocessor producer continue successfully to create newer and improved version of the microprocessor:

a. Intel
b. Motorola
c. Both A and B
d. None of these

75. Motorola has declined how many % share of the microprocessor market to a much smaller share:

a. 50%
b. 55%
c. 48%
d. 51%

76. Which year Intel corporation introduced an updated version of the 8080- the 8085:

a. 1965
b. 1976
c. 1977
d. 1985

77. In 1977 which corporation introduced an updated version of the 8080- the 8085:

a. Motorola
b. Intel
c. Rockwell
d. National

78. How many bit microprocessor developed by Intel:

a. 4 bit
b. 8 bit
c. 32 bit
d. 64 bit

79. Which is the main feature of 8085:

a. Internal clock generator
b. Internal system controller
c. Higher clock frequency
d. All of these

80. Which is 16 Bit microprocessor:

a. 8088
b. 8086
c. 8085
d. All of these

81. How many speed of 8088,8085,8086 microprocessor:

a. 2.5 Million instruction per second
b. 1.5 Million instruction per second
c. 3.5 Million instruction per second
d. 1.6 Million instruction per second

82. Which year Intel family ensured:

a. 1965
b. 1978
c. 1981
d. 1999

83. Which corporation decided to use 8088 microprocessor in personal computer:

a. IBM
b. CRT
c. PMN
d. SPS

84. Which processor provided 1 MB memory:

a. 16-bit 8086 and 8088
b. 32-bit 8086 and 8088
c. 64-bit 8086 and 8088
d. 8-bit 8086 and 8088

85. Who was introduce the 80286 microprocessor updated on 8086,in 1983:

a. Intel
b. Motorola
c. Fairchild
d. None of these

86. Which is the microprocessor launched by Intel:

a. Z-8
b. 8080
c. 8000
d. None of these

87. Which is the microprocessor launched by national semiconductor:

a. IMP-4
b. IMP-8

c. IMP-6
d. IMP-7

88. Which is the microprocessor launched by Rockwell international:

a. RPS-4
b. RPS-6
c. RPS-8
d. All of these

89. Which is the microprocessor launched by Zilog:

a. Z-2
b. Z-4
c. Z-6
d. Z-8

90. CAD stands for:

a. Computer aided drafting
b. Compare aided drafting
c. Both A and B
d. None of these

91. GUI stands for:

a. Graphical user interface
b. Graph used Intel
c. Graphical use inter
d. None of these

92. VGA stands for:

a. Visual graph area
b. Visual graphics array
c. Visual graph accept
d. All of these

93. Pentium Pro Processor contains:

a. L1 Cache
b. L2 Cache
c. Both L1 & L2
d. None of these

94. L1 cache memory is places at _____

a. On Processor
b. On Mother Board
c. On Memory
d. All of these

95. L2 cache memory is places at _____

a. On Processor
b. On Mother Board
c. On Memory
d. All of these

96. Pentium Pro can address _____ of memory:

a. 4 GB
b. 128 GB
c. 256 GB
d. 512 GB

97. Which is the professional or Business version of Intel Processors:

a. Pentium II
b. Pentium Pro
c. Pentium MMX
d. Pentium Xeon

98. Pentium III processor is released in the form of:
a. Socket 370 Version
b. Slot 1 Version in Plastic Cartridge
c. Both a and b

d. None of these

99. What is the maximum clock speed of P III processors

a. 1.0 GHz

b. 1.1 GHz

c. 1.2 GHz

d. 1.3 GHz

100. Power PC microprocessor architecture is developed by:

a. Apple

b. IBM

c. Motorola

d. All of these

101. Which is not the main architectural feature of Power PC:

a. It is not based on RISC

b. Superscalar implementation

c. Both 32 & 64 Bit

d. Paged Memory management architecture

102. Alpha AXP is developed by:

a. DEC

b. IBM

c. Motorola

d. Intel

103. Which is not the main feature of DEC Alpha:

a. 64 Bit RISC processor

b. Designed to replace 32 VAX(CISC)

c. Seven stage split integer/floating point pipeline

d. Variable Instruction length

104. Which is not the open-source OS:

a. Debian

b. BSD Unix

c. Gentoo & Red Hat Linux

d. Windows

105. ISA stands for:

a. Instruct set area
b. Instruction set architecture
c. Both a and b
d. None of these

106. RISC stands for:

a. Reduced Instruction set computer
b. Reduced Instruct set compare
c. Reduced instruction stands computer
d. All of these

107. DEC stands for:

a. Digital electronic computer

b. Digital electronic corporation
c. Digital equipment corporation
d. None of these

108. How many architectural paradigms in microprocessor:

a. 2
b. 3
c. 4
d. 6

109. Which are the architectural paradigms in microprocessor:

a. RISC
b. CISC
c. PISC
d. A and B

110. CISC stands for:

a. Complex instruction set computer
b. Camper instruct set of computer
c. Compared instruction set computer

d. None of these

111. PC's use____ based on this architecture:

a. CPU

b. ALU

c. MU

d. None of these

---

1. BIU STAND FOR:
   - **a. Bus interface unit**
   - b. Bess interface unit
   - c. A and B
   - d. None of these
2. EU STAND FOR:
   - **a. Execution unit**
   - b. Execute unit
   - c. Exchange unit
   - d. None of these
3. The register can be divided are:
   - a. 3
   - **b. 4**
   - c. 5
   - d. 6
4. Which are the part of architecture of 8086:
   - a. The bus interface unit
   - b. The execution unit
   - **c. Both A and B**
   - d. None of these
5. Which are the four categories of registers:
   - a. General- purpose register
   - b. Pointer or index registers
   - c. Segment registers
   - d. Other register
   - **e. All of these**
6. Eight of the register are known as:
   - **a. General- purpose register**
   - b. Pointer or index registers
   - c. Segment registers
   - d. Other register

7. The four index register can be used for:
   - **a. Arithmetic operation**
   - b. Multipulation operation
   - c. Subtraction operation
   - d. All of these
8. IP Stand for:
   - **a. Instruction pointer**
   - b. Instruction purpose
   - c. Instruction paints
   - d. None of these
9. CS Stand for:
   - **a. Code segment**
   - b. Coot segment
   - c. Cost segment
   - d. Counter segment
10. DS Stand for:
   - **a. Data segment**
   - b. Direct segment
   - c. Declare segment
   - d. Divide segment
11. Which are the segment:
   - a. CS: Code segment
   - b. DS: data segment
   - c. SS: Stack segment
   - d. ES:extra segment
   - **e. All of these**
12. The acculatator is 16 bit wide and is called:
   - **a. AX**
   - b. AH
   - c. AL
   - d. DL
13. The upper 8 bit are called_____:
   - a. BH
   - b. BL
   - **c. AH**
   - d. CH
14. The lower 8 bit are called_____:
   - **a. AL**
   - b. CL

c. BL
d. DL

15. IP stand for:
    a. Industry pointer
    b. Instruction pointer
    c. Index pointer
    d. None of these
16. Which has great important in modular programming:
    a. Stack segment
    b. Queue segment
    c. Array segment
    d. All of these
17. Which register containing the 8086/8088 flag:
    a. Status register
    b. Stack register
    c. Flag register
    d. Stand register
18. Which flag are used to record specific characteristics of arithmetic and logical instructions:
    a. The stack
    b. The stand
    c. The status
    d. The queue
19. How many bits the instruction pointer is wide:
    a. 16 bit
    b. 32 bit
    c. 64 bit
    d. 128 bit
20. How many type of addressing in memory:
    a. Logical address
    b. Physical address
    c. Both A and B
    d. None of these
21. The size of each segment in 8086 is:
    a. 64 kb
    b. 24 kb
    c. 50 kb
    d. 16kb
22. The physical address of memory is :
    a. 20 bit

b. 16 bit
c. 32 bit
d. 64 bit

23. The _____ address of a memory is a 20 bit address for the 8086 microprocessor:
a. Physical
b. Logical
c. Both
d. None of these

24. To provide clarity in case of the status register_____ and _____ placeholders are displayed:
a. Binary
b. Hexadecimal
c. Both
d. None of these

25. The pin configuration of 8086 is available in the_____:
a. 40 pin
b. 50 pin
c. 30 pin
d. 20 pin

26. DIP stand for:
a. Deal inline package
b. Dual inline package
c. Direct inline package
d. Digital inline package

27. PA stand for:
a. Project address
b. Physical address
c. Pin address
d. Pointer address

28. SBA stand for:
a. Segment bus address
b. Segment bit address
c. Segment base address
d. Segment byte address

29. EA stand for:
a. Effective address
b. Electrical address
c. Effect address
d. None of these

30. BP stand for:
    a. Bit pointer
    b. Base pointer
    c. Bus pointer
    d. Byte pointer
31. DI stand for:
    a. Destination index
    b. Defect index
    c. Definition index
    d. Delete index
32. SI stand for:
    a. Stand index
    b. Source index
    c. Segment index
    d. Simple index
33. DS stand for:
    a. Default segment
    b. Defect segment
    c. Delete segment
    d. Definition segment
34. ALE stand for:
    a. Address latch enable
    b. Address light enable
    c. Address lower enable
    d. Address last enable
35. AD stand for:
    a. Address data
    b. Address delete
    c. Address date
    d. Address deal
36. NMI stand for:
    a. Non mask able interrupt
    b. Non mistake interrupt
    c. Both
    d. None of these
37. PC stand for:
    a. program counter
    b. project counter
    c. protect counter

d. planning counter

38. AH stand for:

a. Accumulator high

b. Address high

c. Appropriate high

d. Application high

39. AL stand for:

a. Accumulator low

b. Address low

c. Appropriate low

d. Application low

40. Which are the categorized of flag:

a. Conditional flag

b. Control flag

c. Both a and b

d. None of these

41. Which are the general register:

a. AX: Accumulator

b. BX: Base

c. CX: Count

d. DX: Data

e. All of these

42. _____ is the most important segment and it contains the actual assembly language instruction to be executed by the microprocessor:

a. Data segment

b. Code segment

c. Stack segment

d. Extra segment

43. The offset of a particular segment varies from _____:

a. 000H to FFFH

b. 0000H to FFFFH

c. 00H to FFH

d. 00000H to FFFFFH

44. Which are the factor of cache memory:

a. Architecture of the microprocessor

b. Properties of the programs being executed

c. Size organization of the cache

d. All of these

45. _____ is usually the first level of memory access by the microprocessor:

a. **Cache memory**
b. Data memory
c. Main memory
d. All of these

46. which is the small amount of high- speed memory used to work directly with the microprocessor:

a. **Cache**
b. Case
c. Cost
d. Coos

47. The cache usually gets its data from the_____ whenever the instruction or data is required by the CPU:

a. **Main memory**
b. Case memory
c. Cache memory
d. All of these

48. The amount of information which can be placed at one time in the cache memory is called_____:

a. Circle size
b. **Line size**
c. Wide line size
d. None of these

49. How many type of cache memory:

a. 1
b. 2
c. **3**
d. 4

50. Which is the type of cache memory:

a. Fully associative cache
b. Direct-mapped cache
c. Set-associative cache
d. **All of these**

51. Which memory is used to holds the address of the data stored in the cache :

a. **Associative memory**
b. Case memory
c. Ordinary memory
d. None of these

52. Direct mapping is a _____ to implement cache memory :

a. **Cheaper way**

b. Case way
c. Cache way
d. None of these

53. A fourth bit called the _____:
a. Direct bit
b. Cache bit
c. Valid bit
d. All of these

54. FIFO stand for:
a. First in first other
b. First in first out
c. First in first over
d. None of these

55. Microprocessor reference that are available in the cache are called_____:
a. Cache hits
b. Cache line
c. Cache memory
d. All of these

56. Microprocessor reference that are not available in the cache are called_____:
a. Cache hits
b. Cache line
c. Cache misses
d. Cache memory

57. _____ is the most commonly used cache controller with a number of processor sets:
a. L211 controller
b. L210 controller
c. L214 controller
d. None of these

58. LFB stand for:
a. Line full buffers
b. Line fill buffers
c. Line fan buffers
d. None of these

59. LRB stand for:
a. Line read buffers
b. Line ready buffers
c. Line root buffers
d. Line right buffers

60. EB stand for:

a. Effect buffers
b. Effecting buffers
c. Effection buffers
d. None of these

61. EB stand for:
a. Effect buffers
b. Effecting buffers
c. Effection buffers
d. Eviction buffers

62. WB stand for:
a. Write buffers
b. Written buffers
c. Wrote buffers
d. None of these

63. WA stand for:
a. Write allocate
b. Wrote allocate
c. Way allocate
d. Word allocate

64. In case of direct- mapped cache lower order line address bits are used the access the _____:
a. RAM
b. ROM
c. Directory
d. HDD

65. The index high order bits in the address known as_____:
a. tags
b. label
c. point
d. location
e.

66. The parity bits are used to check that a_____:
a. Two bit error
b. Single bit error
c. Multi bit error
d. None of these

67. Who works as cache on the variable:
a. Register
b. Memory

c. Pointer

d. Segment

68. Second level is a cache on the _____:

a. Main memory

b. RAM

c. Both

d. None of these

69. The memory system is said to be effective if the access time of the cache is close to the effective access time of the_____:

a. ROM

b. RAM

c. HDD

d. Processor

70. Cache is usually the_____ of memory access by the microprocessor:

a. First level

b. Second level

c. Third level

d. Fourth level

71. The principal of working of the cache memory largely depends on which locality:

a. Spatial locality

b. Temporal locality

c. Sequentially

d. All of these

72. Who work as a cache for the page table:

a. TLB

b. TLP

c. LEB

d. WAB

73. Which formula is used to calculate the number of read stall cycles:

a. Reads• Read miss rate • Read miss penalty

b. Write* (Write miss rate * Write miss penalty)+write buffer stalls

c. Memory access * Cache miss rate * Cache miss penalty

d. None of these

74. Which formula is used to calculate the number of write stall cycles:

a. Reads* Read miss rate * Read miss penalty

b. Write• (Write miss rate • Write miss penalty)+write buffer stalls

c. Memory access * Cache miss rate * Cache miss penalty

d. None of these

75. Which formula is used to calculate the number of memory stall cycles:

a. Reads* Read miss rate * Read miss penalty
b. Write* (Write miss rate * Write miss penalty)+write buffer stalls
c. Memory access • Cache miss rate • Cache miss penalty
d. None of these

76. Which causes the microprocessor to immediately terminate its present activity:
a. RESET signal
b. INTERUPT signal
c. Both
d. None of these

77. Which are the cache controller ports:
a. 64-bit AHB-Lite slave ports
b. 64-bit AHB-Lite master ports
c. Both
d. None of these

78. Cache can be controlled _____:
a. 16KB-2MB
b. 17 KB-2MB
c. 18 KB-2MB
d. 19 KB-2MB

79. Which is responsible for all the outside world communication by the microprocessor:
a. BIU
b. PIU
c. TIU
d. LIU
e.

80. INTR: it implies the_____ signal:
a. INTRRUPT REQUEST
b. INTRRUPT RIGHT
c. INTRRUPT RONGH
d. INTRRUPT RESET