20008

2008 PUNJAB TECHANICAL UNIVERSITY

B.E ELECTRONICS AND COMMUNICATIONS

VLSI DESIGN PAPER

TIME: 3 HOUR
MARK: 1000

PART A-(10*2=20 marks)

1. How do you prevent latch up problem?

2. List any two types of layout design rules.

3. Define rise time and fall time.

4. Write an expression for power dissipation in CMOS inverter.

5. Differentiate between conditional and procedural assignment.

6. Why do you require sensitivity list?

7. Draw 2:1 Mux using Transmission gate.

8. What are the different types of programming structure available in PAL?

9. What are the different types of CMOS testing?

10. List any two faults that occur during manufacturing.

PART B-(5*16=80 marks)

11. (a) Explain with neat diagram the SOI process and mention its advantages.

(OR)

(b) (i) How are the circuit elements implemented in IC's?

(ii) Explain about CMOS interconnects with diagram.

12. (a)(i) Derive the expression for DC characteristics of CMOS inverte

(ii) Explain the small signal AC characteristics of MOS transistor.

(b) (i) Derive the equation for threshold voltage of a MOS transistor and threshold voltage in terms of flat band voltage.

(ii) Calculate the threshold voltage for a transistor at 300K for a process with a SiO2 gate oxide with thickness 200A.Assume ?ms =-0.9V;Qfc=0.

13. (a) (i) write a Verilog program for 3 to 8 decoder in gate level description.

(ii) What are the differences between behavioral and RTL modeling?

(OR)

(b) Write a Verilog program for 8 bits full adder using one bit full adder. The one bit full adder should be written in behavioral modeling.

14. (a) (i) Explain neatly the ASIC design flow.

(ii) Briefly discuss about different types of ASIC.

(OR)

(b) (i) Implement the following functions using CMOS f(A,B,C)=A'BC+AB'C+ABC'

(ii)Explain the programmable logic structure available in PAL.

15. (a) Briefly explain the system level test technique with neat diagram.

(OR)

(b) Explain with diagram the design strategies for testing the CMOS devices.