CODE NO : RO531O2O1

2008 JAWAHARLAL NEHRU UNIVERSITY [JNU]

III B.TECH I SEMESTER SUPPLIMENTARY EXAMINATIONS

COMPUTER ORGANIZATIONS

(COMMON ELECTRICAL & ELECTRONIC ENGINEERING
ELECTRONIC & COMMUNICATION ENGINEERING)

FEBRU 2008

TIME : 3 HOUR
MARK : 80

ANSWER ANY FIVE QUESTIONS ALL QUESTIONS CARRY EQUAL MARKS

1. (a) Explain the terms computer architecture, computer organization and computer design in a detailed fashion.

(b) Explain about MIPS, FLOPS rating of a processor. How do we arrive at these values.

2. (a) What is the use of buffers. Explain about tri-state buffers. Explain about high impedance state.

(b) Explain commonly employed bit shift operators such as shift left, right, circular shift left/right and arithmetic shift left/right. Assume an 8-bit register, give an example for each

3. (a) Explain the variety of techniques available for sequencing of microinstructions based on the format of the address information in the microinstruction.

(b) Hardwired control unit is faster than microprogammed control unit. Justify this statement.

4. Draw a flowchart to explain how two IEEE 754 floating point numbers can be added, subtracted and multiplied. Assume single precision numbers. Give example for each

5. (a) "In paged segmentation, the reference time increases and fragmentation de- creases", Justify your answer.

(b) A Virtual Memory System has an address space of 8K words and a Memory space of 4K words and page and block sizes of 1K words. Determine the number of page faults for the following page replacement algorithms: 1) FIFO

2) LRU if the reference string is as follows: 4,2,0,1,2,6,1,4,0,1,0,2,3,5,7.

6. (a) Explain bit oriented and character oriented protocols in serial communication.

(b) What are the different issues behind serial communication? Explain.

7. (a) What is pipeline? Explain.

(b) Explain arithmetic pipeline.

8. What is cache coherence and why is it important in shared memory multiprocessor systems? How can the problem be solved with a snoopy cache controller?