GATE CS Topic wise Questions

Computer Organization and Architecture

YEAR 2001

Question. 1

More than one word are put in one cache block to

(A) Exploit the temporal locality of reference in a program

(B) Exploit the spatial locality of reference in a program

(C) Reduce the miss penalty

(D) None of the above

SOLUTION

Cache is the small memory which has a very less access time. So it is used for temporal locality of reference whereas virtual memory is for spatial locality of reference.

Hence (A) is correct option.

Question. 2

A low memory can be connected to 8085 by using

(A) INTER (B) $\overline{\text{RESET IN}}$

(C) HOLD (D) READY

SOLUTION

A low memory can be connected to 8085 by using READY signal. If READY is set then communication is possible.

Hence (D) is correct option.

Question. 3

Suppose a processor does not have any stack pointer register. Which of the following statements is true ?

(A) It cannot have subroutine call instruction

(B) It can have subroutine call instruction, but no nested subroutine calls.

(C) Nested subroutine calls are possible, but interrupts are not.

(D) All sequences of subroutine calls and also interrupts are possible

SOLUTION

Stack pointer register holds the address of top of stack, which is the location of memory at which the CPU should resume its execution after servicing some interrupt or subroutine call.
So if SP register not available then no subroutine call instructions are possible.
Hence (A) is correct option.

Question. 4

A processor needs software interrupt to

(A) Test the interrupt system of the processor.

(B) Implement co-routines.

(C) Obtain system services which need execution of privileged instructions.

(D) Return from subroutine.

SOLUTION

A CPU needs software interrupt to obtain system services which need execution of privileged instructions.
Hence (C) is correct opton.

Question. 5

A CPU has two modes-privileged and non-privileged. In order to change the mode from privileged to non-privileged.

(A) A hardware interrupt is needed.

(B) A software interrupt is needed.

(C) A privileged instruction (which does not generate an interrupt) is needed.

(D) A non-privileged instruction (Which does not generate an interrupt) is needed.

SOLUTION

A software interrupt is initiated by some program module which need some CPU services, at that time the two modes can be interchanged. Hence (B) is correct option.

Question. 6

The process of assigning load addresses to the various parts of the program and adjusting the code and date in the program to reflect the assigned addresses is called

(A) Assembly
(B) Parsing
(C) Relocation
(D) Symbol resolution

SOLUTION

Load addresses are assigned to various parts of the program, the program can be loaded at any location in memory. This location is added to all addresses in the code, to get correct references.
This makes a code re-locatable.
Hence (C) is correct option.

Question. 7

Which of the following requires a device driver ?

(A) Register
(B) Cache
(C) Main memory
(D) Disk

SOLUTION

Device driver is the program which co-ordinates with CPU to regulate the devices. Register, cache & main memory are directly connected to CPU.
So only Disk from given options require device drivers.
Hence (D) is correct option.

Question. 8

Which is the most appropriate match for the items in the first column with the items in the second column

(X.) Indirect Addressing	(I.) Array implementation
(Y.) Indexed Addressing	(II.) Writing re-locatable code
(Z.) Base Register Addressing	(III.) Passing array as parameter

(A) (X, III) (Y, I) (Z, II)

(B) (X, II) (Y, III) (Z, I)

(C) (X, III) (Y, II) (Z, I)

(D) (X, I) (Y, III) (Z, II)

SOLUTION

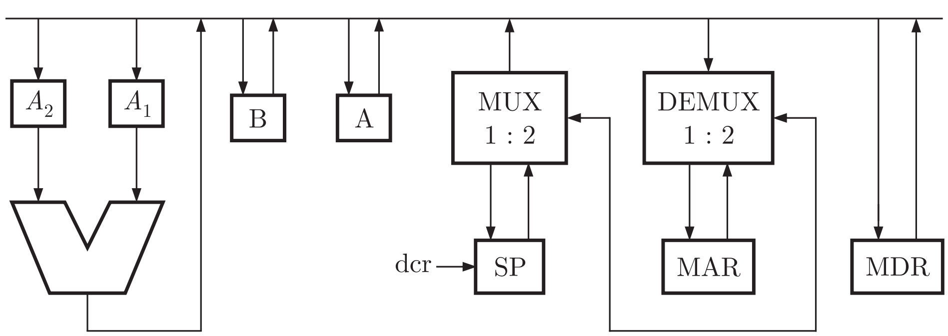
Indexed addressing is used for array implementation where each element has indexes. Base register is used to re-locatable code, where starts from base address & then all local addresses as added to base address.

Indirect addressing is done when array is passed as parameter only name is passed.

Hence (A) is correct option.

Question. 9

Consider the following data path of a simple non-pilelined CPU. The registers A, B, A_1, A_2, MDR the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size 8 × (2:1) and the DEMUX is of size 8 × (1:2). Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and MDR (Memory Date Register). SP can be decremented locally.



The CPU instruction "push r", where = A or B, has the specification

$M[SP] \leftarrow$r

$$SP \leftarrow SP - 1$$

How many CPU clock cycles are needed to execute the "push r" instruction ?

(A) 2 (B) 3

(C) 4 (D) 5

SOLUTION

Push 'r'
Consist of following operations

$$M[SP] \leftarrow r$$
$$SP \leftarrow SP - 1$$

'r' is stored at memory at address stack pointer currently is, this take 2 clock cycles.
SP is then decremented to point to next top of stack.

So total cycles = 3

Hence (B) is correct option.

Question. 10

Which of the following does not interrupt a running process ?

(A) A device (B) Timer

(C) Scheduler process (D) Power failure

SOLUTION

A device can request interrupt service. A timer when finishes or power failure causes a running process to stop. But a scheduler process doesn't do this.
Hence (C) is correct option.

YEAR 2002

Question. 11

A device employing INTR line for device interrupt puts the CALL instruction on the data bus while

(A) $\overline{INTA}$ is active (B) HOLD is active

(C) READY is active (D) None of the above

SOLUTION

INTR is a signal which if enabled then microprocessor has interrupt enabled it receives high INR signal & activates $\overline{INTA}$ signal, so another request can't be accepted till CPU is busy in servicing interrupt.
Hence (A) is correct option.

Question. 12

In 8085 which of the following modifies the program counter ?

(A) Only PCHL instruction

(B) Only ADD instructions

(C) Only JMP and CALL instructions

(D) All instructions

SOLUTION

Program counter is the register which has the next location of the program to be executed next. JMP & CALL changes the value of PC. PCHL instruction copies content of registers H & L to PC.
ADD instruction after completion increments program counter. So program counter is modified in all cases.
Hence (D) is correct option.

Question. 13

In serial data transmission, every byte of data is padded with a '0' in the beginning and one or two '1's at the end of byte because

(A) Receiver is to be synchronized for byte reception

(B) Receiver recovers lost '0's and '1' from these padded bits

(C) Padded bits are useful in parity computation.

(D) None of the above

SOLUTION

In serial data transmission the sender & receiver needs to be synchronized with each other. Receiver should know when 1 byte of data has been sent. 0 & 1's which are padded tell the receiver to synchronize.
Hence (A) is correct option.

Question. 14

Which of the following is not a form of memory ?

(A) Instruction cache (B) Instruction register

(C) Instruction opcode (D) Translation-a-side buffer

SOLUTION

Instruction register stores instruction, look-a-side buffer & instruction cache are also memory.
But instruction opcodes are the opcodes related to an instruction which are not part of memory hierarchy.
Hence (C) is correct option.

Question. 15

In the C language

(A) At most one activation record exists between the current activation record and the activation record for the main.

(B) The number of activation records between the current activation record and the activation record for the main depends on the actual function calling sequence.

(C) The visibility of global variables depends on the actual function calling sequence.

(D) Recursion requires the activation record for the recursive function to be saved on a different stack before the recursive fraction can be called.

SOLUTION

Activation record is the contiguous memory locations where the data needed by the program is kept so at most one activation record exist between current activation record & the record for the main.
Hence (A) is correct option.

Question. 16

In the absolute the addressing mode

(A) The operand is inside the instruction

(B) The address of the operand is inside the instruction

(C) The register containing the address of the operand is specified inside the instruction

(D) The location of the operand is implicit

SOLUTION

In absolute addressing mode, no need of giving operand, the operand are implicit, instruction itself has knowledge of operands.
Hence (D) is correct option.

Question. 17

The performance of a pipelined processor suffers if

(A) The pipelined stages have different delays

(B) Consecutive instructions are dependent on each other

(C) The pipeline stages share hardware resources

(D) All the above

SOLUTION

Pipelining is a method to execute a program breaking it in several independent sequence of stages.
In that case pipeline stages can't have different delays, no dependency among consecutive instructions & sharing of hardware resources shouldn't be there. So option (D) is true
Hence (D) is correct option.

Question. 18

Horizontal microprogramming

(A) Does not require use of signal decoders

(B) Results in larger sized microinstructions than vertical microprogramming

(C) Uses one bit for each control signal

(D) All of the above

SOLUTION

In horizontal microprogramming the instruction size is not large, & no decoding is required. But 1 bit is used for all control signals.
Hence (C) is correct option.

YEAR 2003

Question. 19

For a pipelined CPU with a single ALU, consider the following situations

1. The $j+1-st$ instruction uses the result of $j-th$ instruction as an operand

2. The execution of a conditional jump instruction

3. The $j-th$ and $j+1-st$ instructions require the ALU at the same time

Which of the above can cause a hazard?

(A) 1 and 2 only (B) 2 and 3 only

(C) 3 only (D) All the three

SOLUTION

Case 1 is here of data dependency, this can't be safe with single ALU so read after write.

Case 2 Conditional jumps are always hazardous they create conditional dependency in pipeline

Case 3 This is write after read problem or concurrency dependency so hazardous

All the three are hazardous.

Hence (D) is correct option.

Question. 20

Consider an array multiplier for multiplying two n bit numbers. If each gate in the circuit has a unit delay, the total delay of the multiplier is

(A) $\Theta(1)$ (B) $\Theta(\log n)$

(C) $\Theta(n)$ (D) $\Theta(n^2)$

SOLUTION

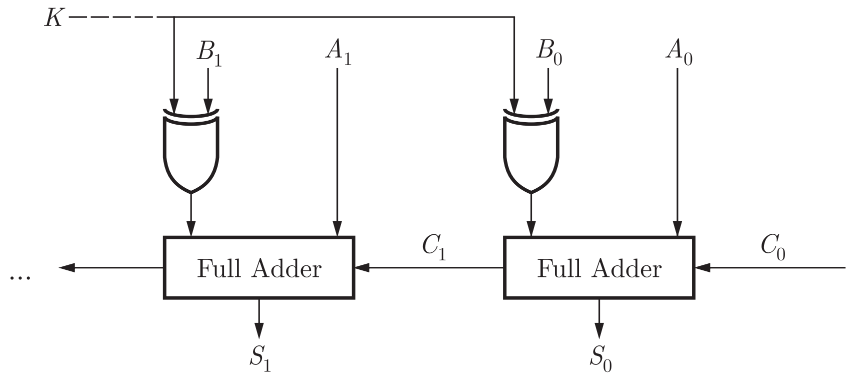
The no. of gates used in n bit array multiplier $(n \times n)$ is $2n-1$. So. if every single gate takes unit delay, then total delay $0(2n-1) = 0(n)$

It is of linear order

Hence (C) is correct option.

Question. 21

Consider the ALU shown below



If the operands are in 2's complement representation, which of the following operations can be performed by suitably setting the control lines K and C_0 only (+ and - denote addition and subtraction respectively)?

(A) $A+B$, and $A-B$,but not $A+1$

(B) $A+B$,and $A+1$,but not $A-B$

(C) $A+B$,but not $A-B$,or $A+1$

(D) $A+B$,and $A-B$,and $A+1$

SOLUTION

This is the ckt to add two numbers in 2's complement form. K & C_0 are set to 1. So $A+B$ & $A-B$ using bit adders can be done. Also since $C_0=1$ & in case B_0, B_1........ all are 0 then it gives $A+1$.
Hence (D) is correct option.

Data for Q. 22 & 23 are given below.

Consider the following assembly language program for a hypothetical processor. A,B and C are 8 bit registers. The meanings of various instructions are shown as comments.

```
     MOV B, # 0     ; B←0
     MOV C, # 8     ; C←8
Z:   CMP C, # 0     ; compare C with 0
     JZX            ; jump to X if zero flag is set
     SUB C, # 1     ; C←C−1
```

```
      RRC A, # 1      ; right rotate A through carry
                      ; by one bit. Thus: if the
                      ; initial values of A and the
                      ; carry flag are a7.......a0 and c0
                      ; respectively, their values
                      ; after the execution of this
                      ; instruction will be c0 a7.....a1
                      ; and a0 respectively.
      JCY             ;jump to Y if carry flag is set
      JMP Z           ; jump to Z
Y:    ADD B, # 1      ; B←B+1
      JMP Z           ; jump to Z
X:
```

Question. 22

If the initial value of register A is A_0, the value of register B after the program execution will be

(A) the number of 0 bits in A_0

(B) the number of 1 bits in A_0

(C) A_0

(D) 8

SOLUTION

Here value of B incremented by 1 only if carry flag is 1, carry is filled using right rotation, so B will store the no. of is in A_0.
Hence (B) is correct option.

Question. 23

Which of the following instructions when inserted at location X will ensure that the value of register A after program execution is the same as its initial value?

(A) $RRC\ A,\#\ 1$

(B) NOP ; no operation

(C) $LRC\ A,\#\ 1$; left rotate A through carry flag by one bit

(D) $ADD\ A,\#\ 1$

SOLUTION

In the end of program execution to check whether both initial and final value of register A is A_0, we need to right rotate register A through carry by one bit.
Hence (A) is correct option.

YEAR 2004

Question. 24

Which of the following addressing modes are suitable for program relocation at run time?

1. Absolute addressing

2. Based addressing

3. Relative addressing

4. Indirect addressing

(A) 1 and 4 (B) 1 and 2

(C) 2 and 3 (D) 1,2 and 4

SOLUTION

Program relocation at run time transfers complete block to some memory locations. This require as base address and block should be relatively addressed through this base address.
This require both based addressing and relative addressing mode.
Hence (C) is correct option.

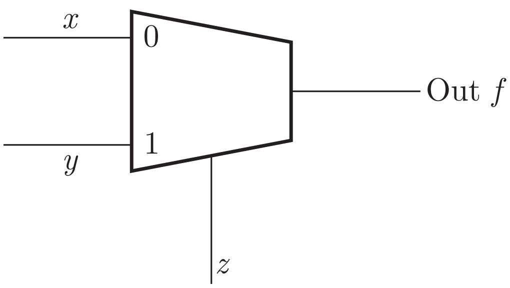
Question. 25

Consider a multiplexer with X and Y as data inputs and Z as control input. $Z = 0$ selects input X, and Z=1 selects input Y. What are the connection required to realize the 2-variable Boolean function $f = T + R$, without using any additional hardware?

(A) R to X, 1 to Y, T to Z (B) T to X, R to Y, T to Z

(C) T to X, R to Y, 0 to Z (D) R to X, 0 to Y, T to Z

SOLUTION

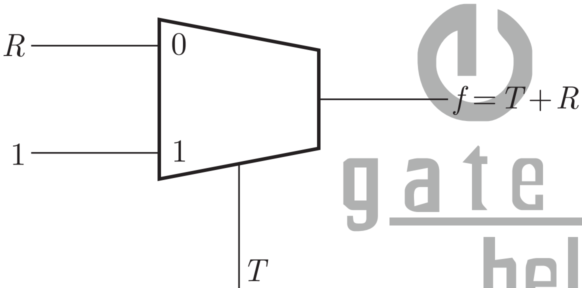


We require $f = T + R$

We have MUX equation

$$f = Z'x + zy$$

Now if we make following ckt



Truth table			
R	T	F	Z
0	0	0	0
0	1	1	1
1	0	1	0
1	1	1	1

So $X = R$ $Y = 1$ $Z = T$

$$f = T'R + T$$
$$= (T + T')(T + R)$$
$$f = T + R$$

Hence (A) is correct option.

Data for Q. 26 & 27 are given below.

Consider the following program segment for a hypothetical CPU having three user registers R1,R2 and R3.

Instruction	Operation	Instruction Size (in words)
MOV R1,5000	;R1←Memory[5000]	2
MOV R2,R3	;R2←R2+R3	1
ADD R2,R3	;R2←R2+R3	1
MOV 6000,R2	;Memory[6000]←R2	2
HALT	;Machine halts	1

Question. 26

Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be

(A) 1007
(B) 1020
(C) 1024
(D) 1028

SOLUTION

Byte addressable so 1 word require 4 bytes.

Instruction no.	Size	Address range
1	2	1000-1007
2	1	1008-1011
3	1	1012-1015
4	2	1016-1023
5	1	1024-1027

Next location 1028.

CPU has executed the HALT instruction so next time the CPU will resume at next location i.e. 1028 which would be at the top of stack.

Hence (D) is correct option.

Question. 27

Let the clock cycles required for various operations be as follows:

Register to/from memory transfer: 3 clock cycles

ADD with both operands in register: 1 clock cycle

Instruction fetch and decode: 2 clock cycles per word

The total number of clock cycles required to execute the program is

(A) 29 (B) 24

(C) 23 (D) 20

SOLUTION

The clock cycles are per block so if an instruction size is 2 then it requires twice no. of clock cycles.

Instruction No.	Size	No. of clock cycles	
1	2	$3 \times 2 + 2$	8
2	1	$1 \times 3 + 2$	5
3	1	1 (add only)	1
4	2	$3 \times 2 + 2$	8
5	1	2 (fetch & decode)	2
Total			24

Hence (B) is correct option.

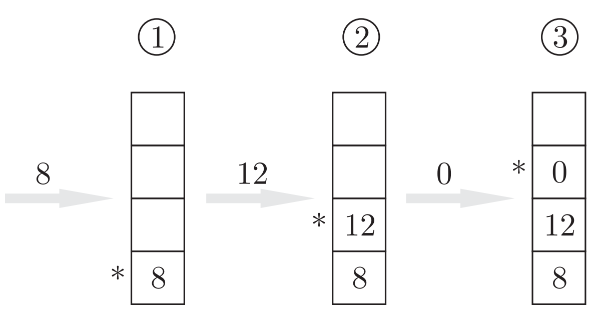
Question. 28

Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is 8, 12,0, 12,8

(A) 2 (B) 3

(C) 4 (D) 5

SOLUTION



After than 12 & 8 are referred but this does not cause any miss

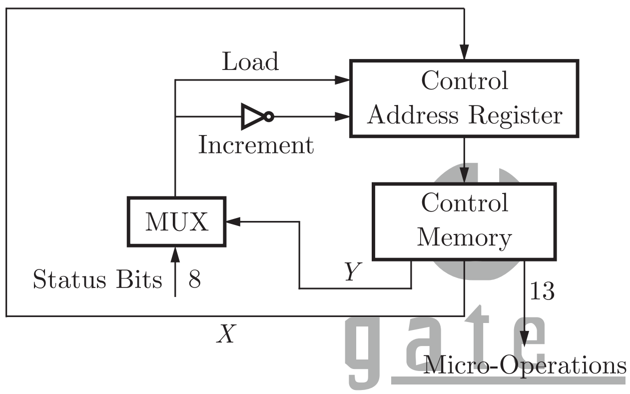
So no. of miss = 3

This stars (*) shows the misses.

Hence (B) is correct option.

Question. 29

The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX.



How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

(A) 10, 3, 1024
(B) 8, 5, 256
(C) 5, 8, 2048
(D) 10, 3, 512

SOLUTION

MUX has 8 states bits as input lines so we require 3 select inputs to select & input lines.

No. of bits in control memory next address field

$$= 26 - 13 - 3$$
$$= 10$$

10 bit addressing, we have 2^{10} memory size.

So X, Y size $= 10, 3, 1024$

Hence (A) is correct option.

Question. 30

A hard disk with a transfer rate of 10 M bytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz. and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?

(A) 5.0%
(B) 1.0%
(C) 0.5%
(D) 0.1%

SOLUTION

$$\text{Transfer rate} = 10 \text{ MB ps}$$
$$\text{Data} = 20 \text{ KB}$$
$$\text{Time} = \frac{20 \times 2^{10}}{10 \times 2^{20}} = 2 \times 10^{-3}$$
$$= 2 \text{ ms}$$
$$\text{Processor speed} = 600 \text{ MHz}$$
$$= 600 \text{ cycles/sec.}$$
$$\text{Cycles required by CPU} = 300 + 900$$
$$\text{For DMA} = 1200$$
$$\text{So time} = \frac{1200}{600 \times 10^6} = .002 \text{ ms}$$
$$\% = \frac{.002}{2} \times 100$$
$$= 0.1\%$$

Hence (D) is correct.

Question. 31

A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be

(A) 120.4 microseconds
(B) 160.5 microseconds
(C) 165.5 microseconds
(D) 590.0 microseconds

SOLUTION

$$\text{Delay} = 5 \text{ ns/stage}$$

Total delay in pipline.

$$= 150 + 120 + 160 + 140 = 570$$

Delay due to 4 stages.

Stage 1 delay 1 stage 2 delay 2 stage 3 stage 4

$$5 \times 3 = 15$$

$$\text{Total} = 570 + 15 = 585$$

$$\text{Total time} = \frac{1000 \text{ data items}}{585 \text{ ns}}$$

$$= 165.5 \text{ microseconds.}$$

Hence (C) is correct option

YEAR 2005

Question. 32

Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line?

(A) Neither vectored interrupt nor multiple interrupting devices are possible

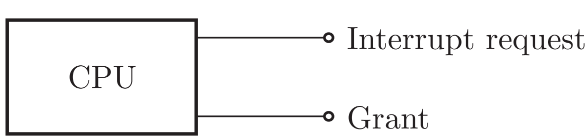
(B) Vectored interrupts are not possible but multiple interrupting devices are possible

(C) vectored interrupts and multiple interrupting devices are both possible

(D) vectored interrupt is possible but multiple interrupting devices are not possible

SOLUTION

CPU has single interrupt request and grant line



Here multiple request can be given to CPU but CPU interrupts only for highest priority interrupt so option (A) & (D) are wrong.

But here in case of single interrupt lines definitely vectored interrupts are not possible.

Hence (B) is correct option.

Question. 33

Normally user programs are prevented from handing I/O directly by I/O instructions in them. For CPUs having explicit I/O instructions, such I/O protection is ensured by having the I/O instructions privileged. In a CPU with memory mapped I/O, there is no explicit I/O instruction. Which one of the following is true for a CPU with memory mapped I/O?

(A) I/O protection is ensured by operating system routine(s)

(B) I/O protection is ensured by a hardware trap

(C) I/O protection is ensured during system configuration

(D) I/O protection is not possible

SOLUTION

In memory mapped I/0 the complete system (memory + I/0 ports) hold the same set of addresses. They are considered to be the part of that memory only. This management is done by OS only.
Hence (A) is correct option.

Question. 34

What is the swap apace in the disk used for?

(A) Saving temporary html pages

(B) Saving process data

(C) Storing the super-block

(D) Storing device drivers

SOLUTION

Swap space is the memory pre allowed to store process's data. This can be compared with virtual memory. The data required to complete process is kept here.
Hence (B) is correct option.

Question. 35

Increasing the RAM of a computer typically improves performance because

(A) Virtual memory increases

(B) Larger RAMs are faster

(C) Fewer page faults occur

(D) Fewer segmentation faults occur

SOLUTION

Due to increase in RAM size all the pages required by CPU are available in RAM so page fault chance are less, so virtual memory access chances are less and latency is reduced for secondary memory.
Hence (C) is correct option.

Question. 36

Consider a three word machine instruction

$$ADD\ A[R_0], @B$$

The first operand (destination) "$A[R0]$" uses indexed addressing mode with $R0$ as the index register. The second operand (source) "$@B$" uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is

(A) 3 (B) 4

(C) 5 (D) 6

SOLUTION

ADD $A[R_0], @B$
This is instruction has 3 computational parts. ADD instruction requires 1 machine cycle, $A[R_0]$ here R_0 is index register which has starting address of index then this index has the block address. This whole operation require 3 machine cycles. Now @ B is indirect addressing. This takes 2 machine cycles. So overall $1 + 3 + 2 = 6$ machine cycles.
Hence (D) is correct option.

Question. 37

Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I	**List-II**
A. $A[1] = B[j]$;	**1.** Indirect addressing
B. while [* A++];	**2.** Indexed addressing
C. int temp=*x;	**3.** Auto increment

Codes:

	A	**B**	**C**
(A)	3	2	1
(B)	1	3	2
(C)	2	3	1
(D)	1	2	3

SOLUTION

LIST-I	LIST-II
A. $A[1] = B[J]$;	2 Indexed addressing here the indexing is used
B. While [$*$ A++]	3. Auto increment the memory locations is A are automatically incriminated.
C. int temp= $*$ X	1. Indirect addressing here temp is assigned the value of int type stored at the address contained in X

A2
B3
C1

Hence (C) is correct option.

Question. 38

Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively

(A) 10,17 (B) 10,22

(C) 15,17 (D) 5,17

SOLUTION

Cache is direct mapped.

$$\text{Size of Cache} = 32 \text{ KB} = 2^5 \times 2^{10} \text{ B} = 2^{15} \text{ Bytes.}$$

Require 15 bits for cache addressing so CPU address has tag and index

$$\text{No. of tag bits} = 32 - 15 = 17$$

From 15 Cache addressing bits consist of blocks & words. Each block has 32 words (bytes) So require 5 bit.

$$\text{Index} = \text{block} + \text{word}$$
$$\text{Block} = 15 - 5 = 10$$

So, 10, 17

Hence (A) is correct option.

Question. 39

A 5 stage pipelined CPU has the following sequence of stages

IF-Instruction fetch from instruction memory.

RD-Instruction decode and register read,

EX- Execute:ALU operation for data and address computation,

MA-Data memory access-for write access the register read at

RD stage it used,

WB-register write back.

Consider the following sequence of instruction:

$$I_1 : LR0, \text{Locl};\ R0 <= M[\text{Locl}]$$
$$I_2\quad AR0, R0;\ R0 <= R0 + R0$$
$$I_3\quad AR2, R0;\ R2 <= R2 - R0$$

Let each stage take one clock cycle.

What is the number of clock cycles taken to complete the above sequence of instruction starting from the fetch of I_1?

(A) 8 (B) 10
(C) 12 (D) 15

SOLUTION

Order of phase in instruction cycle.
$IF \rightarrow A \triangle \rightarrow E \times MA \rightarrow WB$

	1	2	3	4	5	6	7	8	9	10
$R_0 \leftarrow M[LOC]$	IF	RD	EX	MA	WB					
$R_0 \leftarrow R_0 + R_0$			IF	RD	EX	MA	WB			
$R_2 \leftarrow R_2 - R_0$						IF	RD	EX	MA	WB

$R_0 \leftarrow R_0 + R_0$ can't start before 3 since R_0 has not been read by I_1.

$R_2 \leftarrow R_2 - R_0$ can't start before 6^{th} since I_2 has not executed $R_0 \leftarrow R_0 + R_0$ till 5^{th} cycle

Total cycles = 10

Hence (B) is correct option.

Question. 40

A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4 μsec.

The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?

(A) 15 (B) 25
(C) 35 (D) 45

SOLUTION

$$\text{Data transfer rate} = 10000 \text{ B/sec}$$
$$\text{Total data} = 25 \times 10^3$$
$$\text{Rate} = 10^4$$
$$\text{Performance gain} = \frac{25}{10^4} \times 100$$
$$= 25\%$$

Hence (B) is correct option.

Question. 41

Consider a disk drive with the following specification

16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 *rpm*. The disk is operated in cycle stealing mode whereby whenever one byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 $n$sec. The maximum percentage of time that the CPU gets blocked during DMA operation is

(A) 10

(B) 25

(C) 40

(D) 50

SOLUTION

$$\text{Disk revolutions} = 3000 \text{ PM or } 50 \text{ RPS}$$

At a time can read in

$$\text{One revolution} = 512 \text{ KB}$$

$$\text{Tracks read/sec} = \frac{2^{19}}{2^{2}} * 50$$

$$= 50 \times 2^{17} \text{ per sec.}$$

$$\text{Interrupt} = .2621 \text{ sec}$$

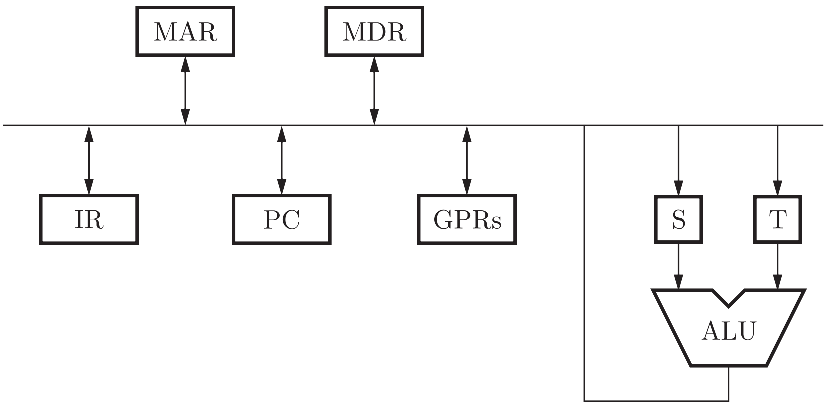
$$\text{Percentage gain} = \frac{.2621}{1} \times 100$$

$$\cong 26\%$$

Hence (B) is correct option.

Data for Q. 42 & 43 are given below

Consider the following data path of a CPU



The, ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycle are needed for memory read operation-the first one for loading data from the memory but into the MDR.

Question. 42

The instruction "add $R0, R1$" has the register transfer in terpretation $R0 <= R0 + R1$. The minimum number of clock cycles needed for execution cycle of this instruction is

(A) 2

(B) 3

(C) 4

(D) 5

SOLUTION

$$R_0 \leftarrow R_0 + R_1$$

First cycle require to fetch operands two cycles required for this.

The next cycle required to use ALU to perform ADD operation.

So total cycles required $= 3$

Hence (D) is correct option.

Question. 43

The instruction "call Rn, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is

$Rn <= PC = 1;$

$PC <= M[PC];$

The minimum number of CPU clock cycles needed during the execution cycle of this instruction is

(A) 2 (B) 3

(C) 4 (D) 5

SOLUTION

$$R_n \leftarrow PC + 1$$
$$PC = M[PC]$$

Program outer is itself a register so incremented in 1 cycle.
Now fetching the memory at PC & the value of at address stored in PC takes 2 cycles.

So total $1 + 2 = 3$ cycles.

Hence (B) is correct option.

Question. 44

A CPU has 24-bit instructions. A program starts at address 300(in decimal). Which one of the following is a legal program counter (all values in decimal)?

(A) 400 (B) 500

(C) 600 (D) 700

SOLUTION

Size of instruction = 24 bits.

Since each instruction require $\frac{24}{3} = 3$ bytes & start address is 300 so the address for this range can be multiple of 3 only so 600.
Hence (C) is correct option.

YEAR 2006

Question. 45

A CPU has a cache with block size 64 bytes. The main memory has k banks, each bank being c bytes wide. Consecutive c-bute chunks are mapped on consecutive banks with warp-around. All the k banks can be accessed in parallel, but two accesses to the same bank must be serialized. A cache block access may involve multiple iterations of parallel bank accesses depending on the amount of data obtained by accessing all the k banks in parallel. Each iteration requires decoding the bank numbers to be accessed in parallel and this takes $k/2$ ns. The latency of one bank access is 80 ns. If $c = 2$ and k=24, then latency of retrieving a cache block starting at address zero from main memory is

(A) 92 ns
(B) 104 ns
(C) 172 ns
(D) 184 ns

SOLUTION

$$\text{Size of Cache block} = 64 \text{ B}$$
$$\text{No. of main memory banks K} = 24$$
$$\text{Size of each bank C} = 2 \text{ bytes.}$$

So time taken for $\|$ access.

$$T = \text{decoding time} + \text{latency time}$$
$$T = \text{K}/2 + \text{latency}$$
$$= 12 + 80$$
$$= 92 \text{ ns.}$$

But since $C = 2$ for accesses.

$$2 \times 92 = 189 \text{ ns.}$$

Hence (D) is correct option

Question. 46

A CPU has five-stages pipeline and runs at 1GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 10^9 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, then total execution time of the program is

(A) 1.0 second
(B) 1.2 seconds
(C) 1.4 seconds
(D) 11.6 seconds

SOLUTION

Given that 80% of 10^9 instruction require single cycle i.e. no conditional branching & for 20% an extra cycle required.

Time taken by 1 cycle $= 10^{-9}$ sec.

$$\text{Total time} = 10^{-9}\left(\frac{80}{100} \times 10^{9} + \frac{20}{100} \times 2 \times 10^{9}\right)$$
$$= 10^{-9} \times 10^{9}\left(\frac{4}{5} + \frac{2}{5}\right)$$
$$= \frac{6}{5} = 1.2 \text{ seconds.}$$

Hence (B) is correct option.

Question. 47

Consider a new instruction named branch-on-bit-set (mnemonic bbs). The instruction "bbs reg, pos, labbel" jumps to label if bit in position pos of register operand reg is one. a register is 32 bits wide and the bits are numbered 0 to 31, bit in position 0 being the least significant. Consider the following emulation of this instruction on a processor that does not have bbs implemented.

temp←reg and mask

Branch to label if temp is non-zero

The variable temp is a temporary register. For correct emulation the variable mask must be generated by

(A) mask← $0x1 << pos$ (B) musk← $0x$ *ffffffff* $>> pos$

(C) mask← pos (D) msdk← $0xf$

SOLUTION

Given instruction
bbs reg, pos, Label
Here pos bit decided whether to jump to label. So all other bits in temp set to 0.

Temp ← reg and mask.

So of temp is not zero branch to label.
So shifting left over.

Mask ← $0 \times 1 <<$ pos

Hence (D) is correct option.

Data for Q. 48 & Q. 49 are given below. Solve the problem and choose the correct answers.

Consider two cache organizations: The first one is 32 KB 2-way set associative with 32-bytes block size. The second one is of the same size but direct mapped. The size of an address is 32 bits in both cases A2-to-1 multiplexes has latency of 0.6 ns where a k-bit comparator has a latency of $k/10ns$. The hit latency of the set associative organization is h_1 while that of the direct mapped one is h_2.

Question. 48

The value of h_1 is

(A) $2.4ns$ (B) $2.3ns$

(C) $1.8ns$ (D) $1.7ns$

SOLUTION

2 way set-associative Cache.

Size 32 KB

2 way so 16 KB sets.

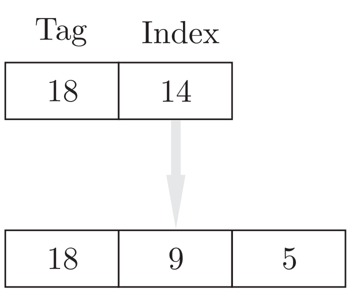
Require 14 bits for 2^{14} B

Block size = 32 Byte.

= 5 bits.

No. of blocks $14 - 5 = 9$

Tag index



$$h_1 = \frac{18}{10} + 0.6 \text{ ns}$$

$$= 2.4 \text{ ns}.$$

Hence (A) is correct option.

Question. 49

The value of h_2 is

(A) $2.4ns$ (B) $2.3ns$

(C) $1.8ns$ (D) $1.7ns$

SOLUTION

Similarly to previous question. The CPU address is same but Direct coaching require for 32 KB 15 bits.

Which would be $10+5=17$

17	10	5

$$h_2 = \frac{17}{10} + 0.6$$

$$= 2.3 \text{ ns}$$

Hence (B) is correct option.

Data for Q. 50 & Q. 51 are given below.

A CPU has a 32 KB direct mapped cache with 128-byte block size. Suppose A is a two dimensional array of size 512×512 with elements that occupy 8-bytes each. Consider the following two C code segments, P_1 and P_2,

```
P1 : for (i=0;i<512;i++)
{
     for (j=0;j<512;j++)
{
          x+=A[i][j];
     }
}
P2 : for (i=0;i<512;i++) {
          for (j=0;j<512;j++) {
     {x+=A[j][i];}
     }
}
```

$P1$ and $P2$are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by $P1$ be M_1 and that for $P2$ be M_2.

Question. 50

The value of M_1 is

(A) 0 (B) 2048

(C) 16384 (D) 262144

SOLUTION

Given loop P_1 accesses array A row wise & P_2 access column wise.

$$M_1 = ?$$
$$\text{Cache Capacity} = 2^{15} \text{ B.}$$
$$1 \text{ element} = 2^3 \text{ B}$$
$$\text{Total elements } 512 \times 512$$
$$\text{Total data} = 512 \times 512 \times 8 \text{ B}$$
$$= 2^{21} \text{ B}$$
$$\text{Block size} = 128 \text{ B}$$
$$1 \text{ block can have} = \frac{128}{8} = 16 \text{ elements}$$
$$\text{So total blocks require} = \frac{512 \times 512}{16}$$
$$= 1638 \text{ blocks}$$

Since the memory is initially empty so all blocks are required at least once.

So, $M_1 = 16384$

Hence (C) is correct option.

Question. 51

The value of the ratio M_1/M_2 is

(A) 0 (B) 1/16

(C) 1/8 (D) -16

SOLUTION

Now $M_2 = ?$

In the case (P_2 loop) the array is accessed column wise, so even the block brought for $A[0][0] - A[0][15]$ would not be used for second column wise access i.e. $A[1][0]$ So new block need to swap, similarly for $A[3][0]$ & So on. This would continue for every element, since memory is contiguous.

So $M_2 = 512 \times 512 = 262144$

& $$\frac{M_1}{M_2} = \frac{16384}{262144} = \frac{1}{16}$$

Hence (B) is correct option.

YEAR 2007

Question. 52

Consider a 4-way set associative cache consisting of 120 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively

(A) 9,6,5 (B) 7,7,6

(C) 7,5,8 (D) 9,5,6

SOLUTION

4 way set associative cache

$$\text{Size} = 128 \times 64 \text{ words}$$

$$\text{But for 4 sets } \frac{128 \times 64}{4} = 32 \times 64$$

For 32 lines we require 5 bits.

For 64 words we require 6 bits.

$$\text{Indexing} = 6 + 5 = 11 \text{ bits.}$$

$$\text{Tag} = 20 - 11$$

$$= 9 \text{ bits}$$

9	5	6

Hence (D) is correct option.

Question. 53

Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively

(A) 256 Mbytes, 19 bits (B) 256 Mbyte, 28 bits

(C) 512 Mbytes, 20 bits (D) 64 Gbyte, 28 bits

SOLUTION

$$\begin{aligned} \text{Surface} &= 6 \\ \text{Tracks} &= 16 \times 128 \\ \text{Sectors} &= 16 \times 128 \times 256 \\ &= 2^4 \times 2^7 \times 2^8 = 2^{19} \end{aligned}$$

So 19 lines are required to address all sectors.

$$\begin{aligned} \text{Bytes} &= 2^{19} \times 512 \text{ B} \\ &= 2^{19} \times 2^9 \\ B &= 2^{28} \\ &= 256 \text{ MB} \end{aligned}$$

Hence (A) is correct option.

Question. 54

Consider a pipelined processor with the following four stages

```
IF: Instruction Fetch
ID: Instruction Decode and Operand Fetch
EX: Execute
WB: Write Bank
```

The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction need 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD	R2,	R1,	R0	R2←R1+R0
MUL	R4,	R3,	R2	R4←R3*R2
SUB	R6,	R5,	R4	R6←R5−R4

(A) 7
(B) 8
(C) 10
(D) 14

SOLUTION

Order of instruction cycle-phases.

$IF \rightarrow ID \rightarrow EX \rightarrow WB$

We have 3 instructions.

	1	2	3	4	5	6	7	8

$R_2 \leftarrow R_1 \leftarrow R_0$	IF	ID	EX	WB				
$R_4 \leftarrow R_3 \leftarrow R_2$		IF	ID	EX	EX	EX	WB	
$R_6 \leftarrow R_5 \leftarrow R_4$			IF	ID	-	-	EX	WB

Represent wait in pipeline due to result dependently.

Clock cycles require $= 8$

Hence (B) is correct option.

Data for Q. 55, 56 & 57 are given below.

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

Instruction	Operation	Instruction size (no. of words)
MOV R1,(3000)	R1←M[3000]	2
LOOP:		
MOV R2,R1	R2←M[R3]	1
ADD R2,R1	R2←R1+R2	1
MOV (R3),R2	M(R3]←R2	1
INC R3	R3←R3+1	1
DEC R1	R1←R1-1	1
BNZ LOOP	Branch on not zero	2
HALT	Stop	

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 100. All the numbers are in decided.

Question. 55

Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

(A) 10
(B) 11
(C) 20
(D) 21

SOLUTION

1^{st} memory reference $R1 \leftarrow M\ [3000]$ and then in the loop which runs for 10 times there are 2 memory reference every iteration.

$$10 \times 2 = 20$$

Total $20 + 1 = 21$

$$R_2 \leftarrow M[R_3]$$

$$M[R_3] \leftarrow R_2$$

Hence (D) is correct option

Question. 56

Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is

(A) 100
(B) 101
(C) 102
(D) 110

SOLUTION

Program stores results from 2000 to 2010. It stores 110, 109, 108......100 at 2010 location.
DEC R1
Hence (A) is correct option.

Question. 57

Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction "INC R3", what return address will be pushed on to the stack?

(A) 1005
(B) 1020
(C) 1024
(D) 1040

SOLUTION

Now byte addressable memory so 1 word i.e. 4 bytes require 4 addresses.

Instruction	Words	Location
MOV R1, (3000)	2	1000-1007
MOV R2, R1	1	1008-1011
ADD R2, R1	1	1012-1015

MOV (R3), R2	1	1016-1019
INC R3	1	1020-1023
DEC R1	1	1024-1027

Interrupt occurs during execution of INC R3, So CPU will complete the execution of this instruction and then Push the next address 1024 to the stack, so after interrupt service the program can be resumed from next instruction.

Hence (C) is correct option.

Data for Q. 58 & Q. 59 are given below.

Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50×50 two-dimensional array of bytes is stored in the main memory stating from memory location 1100H.Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

Question. 58

How many data cache misses will occur in total?

(A) 48
(B) 50
(C) 56
(D) 59

SOLUTION

Size of main memory 2^{16} bytes.

$$\text{Size of Cache} = 32 \times 64 \text{ B}$$
$$= 2^{11} \text{ B}$$
$$\text{Size of array} = 2500 \text{ B}$$

Array is stored in main memory but cache is empty.

$$\text{Size of Cache} = 2048 \text{ B}$$
$$\text{So no. of page faults} = 2500 - 2048$$
$$= 452$$
$$\text{For second access} = 452 \times 2 = 904$$
$$\text{Total} = 1356$$

Hence (C) is correct option.

Question. 59

Which of the following lines of the data cache will be replaced by new blocks in accessing the array

(A) line 4 to line 11 (B) line 4 to line 12

(C) line 0 to line 7 (D) line 0 to line 8

SOLUTION

$$\text{No of page faults} = 452$$
$$\text{One line has } 64 \text{ B}$$

So the line at which these page faults will finish.

$$= \frac{452}{64} \cong 7$$

So 0 to 7 line

Hence (C) is correct option.

YEAR 2008

Question. 60

For a magnetic disk with concentric circular track, the latency is not linearly proportional to the seek distance due to

(A) non-uniform distribution of requests

(B) arm starting and stopping inertia

(C) higher capacity of tracks on the periphery of the platter

(D) use of unfair arm scheduling policies.

SOLUTION

Tracks on magnetic disks are concentric a seek is from me sector to other may or mayn't be in different tracks.

This seek distance is not proportional to latency since the tracks at periphery has higher diameter so high in capacity to store data.

Hence (C) is correct option.

Question. 61

Which of the following is/are true of the auto increment addressing mode?

1. It is useful in creating self relocating code

2. If it is included in an Instruction Set Architecture, then an

additional ALU is required for effective address calculation

3. The amount of increment depends on the size of the data item accessed.

(A) 1 only (B) 2 only

(C) 3 only (D) 2 and 3 only

SOLUTION

In auto increment addressing mode the address where next data block to be stored is generated automatically depending upon the size of single data item required to store. So statement 3 is correct.
Statement says that this mode is used for self relocating code, but this is false since self relocating code, takes always some address in memory.
Statement 2 is also incorrect since no additional ALV is required.
Hence (C) is correct option.

Question. 62

Which of the following must be true for the RFE (Return from Expectation) instruction on a general purpose processor.

1. It must be a trap instruction
2. It must be a privileged instruction
3. An exception can not be allowed to occur during execution of an RFE instruction.

(A) 1 only (B) 2 only

(C) 1 and 2 only (D) 1, 2 and 3 only

SOLUTION

RFE (Return From Exception) is a privileged trap trap instruction which is executed when exception occurs, so an exception is not allowed to execute.
Hence (D) is correct option.

Question. 63

For inclusion to hold between two cache level L1 and L2 in a multilevel cache hierarchy, which of the following are necessary?

1. L1 must be a write-through cache
2. L2 must be write-through cache

3. The associativity of L2 must be greater that of L1
4. The L2 cache must be at least as large as the L1 cache

(A) 4 only (B) 1 and 2 only

(C) 1, 2 and 4 only (D) 1, 2, 3 and 4

SOLUTION

Level 1 ($L1$) & Level 2 ($L2$) cache are placed between CPV & they can be both write through cache but this is not necessary.
Associativity has no dependence but $L2$ cache must be at least as large as $L1$ cache, since all the words in $L1$ are also is $L2$.
Hence (A) is correct option.

Question. 64

Which of the following are NOT true in a pipe lined processor?

1. Bypassing can handle alll Raw hazards.
2. Register renaming can eliminate all register carried WAR hazards.
3. Control hazard penalties can be eliminated by dynamic branch prediction.

(A) 1 and 2 only (B) 1 and 3 only

(C) 2 and 3 only (D) 1,2 and 3

SOLUTION

In a pipelined processor by passing can't handle all the row hazards.
Registers carried WAR doesn't have register naming as proper solution.
And control hazard penalties are eliminated by delayed branching not by dynamic branch prediction.
So all are false.
Hence (D) is correct option.

Question. 65

The use of multiple register windows with overlap causes a reduction in the number of memory accesses for

1. Function locals and parameters

2. Register saves and restores

3. Instruction fetches

(A) 1 only
(B) 2 only
(C) 3 only
(D) 1,2 and 3

SOLUTION

Multiple register windows with overlap causes a reduction in the number of memory accesses for instruction fetching.
Hence (C) is correct option.

Question. 66

In an instruction execution pipeline, the earliest that the data TLB (Translation Look aside Buffer) can be accessed is

(A) before effective address calculation has started

(B) during effective address calculation

(C) after effective address calculation has completed

(D) after data cache lookup has completed

SOLUTION

TLB is used during effective address calculation in an instruction execution pipeline.
Hence (B) is correct option.

Data for Q. 67, 68 & 69 are given below.

Consider a machine a 2-way set associative data cache of size 64 kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addressed and the page size is 4 kbytes. A program to be run on this machine begins as follows:

```
Double APR[1024]]1024]
int i, j;
/*Initalize array APR to 0.0*/
for (i = 0;i < 1024;i ++)
for  (j = 0;k < 1024;j ++)
APR[i] [j] = 0.0;
```

The size of double 8 bytes. Array APR is in memory stating at the beginning of virtual page $0 \times FF000$ and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array APR.

Question. 67

The total size of the tags in the cache directory is

(A) 32 kbits (B) 34 kbits

(C) 64 kbits (D) 68 kbits

SOLUTION

$$\begin{aligned}\text{Virtual (CPU) address has} &= 32 \text{ bits}\\ \text{2 way set associative cache size} &= 64 \text{ KB}\\ \text{Size of 1 set} &= 32 \text{ KB}\end{aligned}$$

Require 15 bits for indexing.

$$\begin{aligned}\text{So Tag} &= 32 - 15 = 17\\ \text{Size of block} &= 16 \text{ bytes}\\ &= 4 \text{ bits are required}\\ \text{Index} &= \text{block} + \text{word}\\ \text{Block} &= 15 - 4 = 11\end{aligned}$$

17	11	4

CPV address

Size of tags = There are 2^{17} bytes of tags in every set of cache.

$$\begin{aligned}\text{So total} &= 17 \times 2 \times 1024\\ &= 34 \text{ KB.}\end{aligned}$$

Hence (B) is correct option.

Question. 68

Which of the following array elements has the same cache index as APR [0][0]?

(A) APR[0][4] (B) APR[4][0]

(C) APR[0][5] (D) APR[5][0]

SOLUTION

Elements stored in row major order. Two elements should have same cache index (15 bits) & their tags may be different (17 bits).

So $APR[\circ][\circ]$ the MSB 17 bits will be changed.

APR[∘][∘] APR[∘][1]...............
APR[2][∘]................................
APR[4][∘]................................

So on.
This is virtual memory storage.
So 15 LSB of APR [∘][∘] & APR [∘][∘] are same so same index APR [∘] & APR [4] 17 MSB are different so tags differ.
Hence (B) is correct option.

Question. 69

The cache hit ratio for this initialization loop is

(A) 0%
(B) 25%
(C) 50%
(D) 75%

SOLUTION

$$\text{Cache hit ratio} = \frac{\text{No. of hits}}{\text{Total accesses}}$$

$$= \frac{1024}{1024 + 1024} = \frac{1}{2} = 0.5$$

or $= 50\%$

Hence (C) is correct option.

Data for Q. 70 & 71 are given below.

Delayed branching can help in the handling of control hazardous

Question. 70

For all delayed conditional branch instruction, irrespective of weather the condition evato true or false, A

(A) the instruction following the conditional branch instruction in memory is executed
(B) the first instruction in the fall through path is executed
(C) the first instruction in the taken path is executed
(D) the branch takes longer to execute that any other instruction

SOLUTION

Delayed branching for conditional instructions, irrespective of whether the condition evaluates to true or false, the first instruction in the fall through path would be executed this prevent from hazardous control transfer.
Hence (B) is correct option.

Question. 71

The following code is to run on a pipe lined processor with one branch delay slot

```
11: ADD  R2 ← R7+R8
12: SUB  R4 ← R5− R6
13: ADD R1 ← R2+ R3
14: STORE Memory [R4] ←  R1
BRANCH to Label if R1==0
```

Which of the instruction 11,12,13 or 14 can legitimately occupy the delay slot without any other program modification?

(A) 11 (B) 12

(C) 13 (D) 14

SOLUTION

In pipelining result of 1 instruction is used for the next in pipeline. Delay slot will be occupied by the next instruction in the fall through path. The branching instruction $R1 == 0$ goto Label X.
So in delay slot I_2 will be there.

Hence (B) is correct option.

YEAR 2009

Question. 72

How many 32K×1 RAM chips are needed to provide a memory capacity of 356-bytes ?

(A) 8 (B) 32

(C) 64 (D) 128

SOLUTION

$$\text{Memory capacity of 1 RAM} = 32 \text{ K bits}$$
$$\text{Total Memory required} = 256 \text{ K bytes}$$
$$\text{No. of RAM} = \frac{256 \times K \times 2^3 \times \text{bits}}{32 \times K \times \text{bits}}$$
$$\text{Chips required} = \frac{2^8 \times 2^3}{2^5}$$
$$= 2^6$$
$$= 64$$

Hence (C) is correct option.

Question. 73

A CPU generally handles are interrupt by executing an interrupt service routine

(A) As soon as an interrupt is raised

(B) By checking the interrupt register at the end of fetch cycle

(C) By checking the interrupt register after finishing the execution of the current instruction

(D) By checking the interrupt register at fixed time intervals

SOLUTION

An interrupt is a signal delivered to CPU, which tells to stop its normal service routine & execute interrupt service routine.
This interrupt service routine is checked as soon as CPU receives the interrupt but since CPU working unit is an instruction so CPU can switch to ISR only after execution of current instruction.
Hence (C) is correct option.

Question. 74

Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions 11, 12, 13, 14 in stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1	2	1	1	1
I2	2	3	2	2
I3	2	1	1	3

I4	1	2	2	2

What is the number of cycles needed to execute the following loop?

for $(i = 1\ to\ 2)\{$I1; I2; I3; I4;$\}$

(A) 16
(B) 23
(C) 28
(D) 30

SOLUTION

We can see a single iteration of given for loop according to the cycles required.

Cycle	S_1	S_2	S_3	S_4	Completion
1	I_1				
2	I_1				
3	I_2	I_1			
4	I_3	I_2	I_1		
5	I_3	I_2		I_1	I_1
6	I_4	I_2			
7		I_3	I_2		
8		I_4	I_2		
9		I_4	I_3	I_2	
10			I_4	I_2	I_2
11			I_4	I_3	
12				I_3	
13				I_3	I_3
14				I_4	
15				I_4	I_4

$$\text{No. of cycle of 2 iteration} = 2 \times 15 = 30$$

Hence (D) is correct option.

Question. 75

Consider a 4 way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks is in the following order :

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155

Which one of the following memory block will NOT be in the cache if LRU replacement policy is used ?

(A) 3 (B) 8

(C) 129 (D) 216

SOLUTION

4 way set associative so 16 block will be divided in 4 sets of 4 blocks each.
We apply (Address mod 4) function to decide set.

Set 0	0	48	0	$\bmod 4 = 0$	*
	4	32	255	$\bmod 4 = 3$	*
	8	8	1	$\bmod 4 = 1$	*
	216	92	4	$\bmod 4 = 0$	*
Set 1	1	1	3	$\bmod 4 = 3$	*
	133	133	8	$\bmod 4 = 0$	*
	129	129	133	$\bmod 4 = 1$	*
	73	73	159	$\bmod 4 = 3$	*
Set 2			216	$\bmod 4 = 0$	*
			129	$\bmod 4 = 1$	*
			63	$\bmod 4 = 3$	*
			8	$\bmod 4 = 0$	*
Set 3	255	155	98	$\bmod 4 = 0$	*
	3	3	32	$\bmod 4 = 0$	*
	159	159	73	$\bmod 4 = 1$	*
	63	63	92	$\bmod 4 = 0$	*
			155	$\bmod 4 = 3$	*

All * are misses $S1$ is the first stage & $S2$ is second.
In the second stage 216 is not present in Cache
Hence (D) is correct option.

Common Data for Question 76 & 77

A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple $\langle c, h, s\rangle$, where c is the cylinder number, h is the surface number and s is the sector number. Thus, the 0^{th} sector is addressed as $\langle 0,0,0\rangle$, the 1st sector as $\langle 0,0,1\rangle$, and so on.

Question. 76

The address $\langle 400,16,29\rangle$, corresponds to sector number:

(A) 505035 (B) 505036

(C) 505037 (D) 505038

SOLUTION

Each cylinder has 10 platters or 20 recording surfaces

$$\text{or } 63 \times 20 \text{ sector} = 1260 \text{ sectors.}$$

Each recording surface has 63 sectors.

So $$< 400, 16, 29 > = < c, h, s >$$

$$400 \times 1260 + 16 \times 63 + 29$$

$$505037$$

Hence (C) is correct option.

Question. 77

The address of 1039^{th} sector is

(A) $\langle 0,15,31\rangle$ (B) $\langle 0,16,30\rangle$

(C) $\langle 0,16,31\rangle$ (D) $\langle 0,17,31\rangle$

SOLUTION

1 cylinder has 1260 sectors

So address for 1039^{th} sector.

$$C = 0$$

Each surface has 63 sectors.

$$\text{Total surface here} = \frac{1039}{63} = 16 \text{ surfaces}$$

Remainder here 31 sectors

So $< 0, 16, 31 >$.

Hence (C) is correct option.

YEAR 2010

Question. 78

A main memory unit with a capacity of 4 megabytes is build using $1\text{M} \times 1 -$ bit DRAM chips. Each DRAM chip has 1K rows of cells with 1 K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is

(A) 100 nanoseconds
(B) $100^{*}2^{10}$nanoseconds
(C) $100^{*}2^{20}$nanoseconds
(D) $3200^{*}2^{20}$nanoseconds

SOLUTION

$$\text{Size of main memory} = 4\text{ MB}$$
$$1\text{ DRAM size} = 1\text{ Mb}$$
$$\text{No. of chips required} = \frac{4 \times M \times 8 \times b}{1 \times M \times b} = 32$$

1 DRAM has 1 K rows
1 ROW has 1 K cells

$$\text{Total cells in 1 DRAM} = K^2 = 2^{20}$$
$$\text{In 32 DRAM} = 32 \times 2^{20}\text{ Cells}$$

1 cell refresh take 100 ns.
So total refresh time

$$= 32 \times 100 \times 2^{20}\text{ ns}$$
$$= 3200 \times 2^{20}\text{ ns.}$$

Hence (D) is correct option.

Question. 79

A-5 stage pipelined processor has Instruction Fetch. (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instruction. The PO stage takes 1 stake clock cycle for ADD and SUB instructions 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions ?

Instruction	Meaning of instruction
I_0: MUL R_2, R_0, R_1	$R_2 \leftarrow R_0 {}^{*} R_1$
I_1: DIV R_5, R_3, R_4	$R_5 \leftarrow R_3/R_4$
I_2: ADD R_2, R_5, R_2	$R_2 \leftarrow R_5 + R_2$
I_3: SUB R_5, R_2, R_6	$R_5 \leftarrow R_2 - R_6$

(A) 13 (B) 15
(C) 17 (D) 19

SOLUTION

The order of operations $IF \rightarrow ID \rightarrow OF \rightarrow PO \rightarrow WO$

Figure

Here $A = (R_3/R_4) + R_2, R_6$

So we can see that all the instruction can be executed in 17 clock cycles using piplining.

Hence (C) is correct option.

Question. 80

The program below uses six temporary variables a, b, c, d, e, f

$a = 1$
$b = 10$
$c = 20$
$d = a + b$
$e = c + d$
$f = c + e$
$b = c + e$
$e = b + f$
$d = 5 + e$

Assuming that all operations take their operands from register, what is the minimum number of registers needed to execute this program without spilling ?

(A) 2 (B) 3
(C) 4 (D) 6

SOLUTION

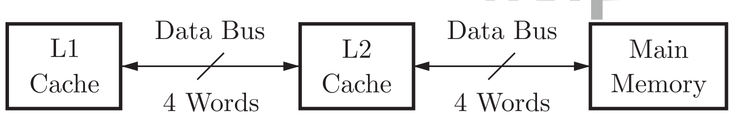
Replacement

R_1	R_2	R_3
a	b	c
d	b	c
d	e	c
f	e	c
f	b	c
f	e	c
f	e	d

So all the operations done using 3 registers only.
Hence (B) is correct option.

Common Data for Questions 81 & 82

A computer system has an L1 and L2 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size is L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unity respectively.



Question. 81

When there is a miss in L1 cache and a hit in L2 cache, a block is transferred form L2 cache to L1 cache. What is the time taken for this transfer ?

(A) 2 nanoseconds (B) 20 nanoseconds

(C) 22 nanoseconds (D) 88 nanoseconds

SOLUTION

Each block is $L2$ Cache is 4 times $L1$ Cache. So far 1 block miss in $L1$ Cache the block from $L2$ to $L1$ will be transferred, but $L2$ block has size 16 words & $L1$ data bus of 4 words, so $4L2$ & $4L1$ access are required.

$$4 \times 2 + 4 \times 20$$
$$8 + 80$$
$$88 \text{ ns}$$

Hence (D) is correct option.

Question. 82

When there is a miss in both L1 cache and L2 cache, first a block is transferred from memory to L2 cache, and then a block is transferred from L2 cache to L1 cache. What is the total time taken for these transfers ?

(A) 222 nanoseconds (B) 888 nanoseconds

(C) 902 nanoseconds (D) 968 nanoseconds

SOLUTION

Miss in both $L1$ & $L2$. Cause main memory to transfer that block in both cache.

1 block of Main memory has 16 words but data bus of $L2$ has only 4 words. So 4 access of Main memory & 4 access of $L2$ Cache required to update $L2$

$$4 \times 20 + 4 \times 200$$
$$80 + 800 = 880 \text{ ns}$$

Now $L2$ updates $L1$, this takes 4 access to $L1$ & 4 access to $L2$

$$4 \times 2 + 4 \times 20$$
$$8 + 80 = 88 \text{ ns}$$
$$\text{Total time} = 880 + 88$$
$$= 968 \text{ ns}$$

Hence (D) is correct option.

****