

ROLLNO.....

**2006 NATIONAL INSTITUTE OF TECHNOLOGY**  
**IV SEMESTER B.TECH DEGREE EXAMINATIONS**  
**PULSE AND DIGITAL CIRCUITS**  
**(EEE)**

NOV 2007

TIME:3 HOUR  
MARK:100

ANSWER ALL THE QUESTIONS

1) The diode in the figure below has a storage time constant of  $3\mu\text{s}$  and transition capacitance of  $1\text{nF}$ . The switch is closed at  $t=15\mu\text{s}$ . Calculate and plot the minority charge storage in the diode, diode current, voltage across diode and voltage across resistor from  $t=0$  to  $t=25\mu\text{s}$ .

2) The input wave in the figure below is a  $200\text{kHz}$  square wave with  $6\text{V}$  high level and  $0\text{V}$  low level. The transistor parameters are  $\beta_{\text{min}} = 70$ ,  $C_{\text{Te}} = 4\text{pF}$ ,  $C_c = 7\text{pF}$ ,  $r_{\text{bb}}' = 30\text{ohms}$ ,  $\tau_s = 350\text{ns}$  and  $f_T = 7.5\text{MHz}$ . Find all the components of switch-off delay and switch-on delay of the transistor and draw the output voltage waveform showing the various switching delay components.

3. Explain why

(i) Standard TTL is faster than standard DTL

(ii) Schottky TTL is faster than standard TTL

(iii) TTL Supply Current contains spikes

(iv) Flip Flops draw more supply current when clock waveform rise and fall times increase

(v) ECL uses negative supply and

(vi) Speed-power product is used as a figure of merit in comparing digital logic families

4. Derive expressions for the rise time and fall time for a CMOS Inverter driving a capacitive load as shown in the figure below. Evaluate the rise time and fall time for  $k_D = 1\text{mA/V}^2$ ,  $k_L = 1.3\text{mA/V}^2$ ,  $V_{\text{Tn}} = 2.5\text{V}$ ,  $V_{\text{Tp}} = 2\text{V}$  and  $C = 1\text{nF}$  assuming an ideal square wave input at the input of the gate.

5(a) Explain how Combinational Logic may be implemented using a ROM. Illustrate the procedure by designing a ROM Implementation for a circuit which accepts a 3-bit number and generates a binary number which is equivalent to  $x^3 + 2$  where  $x$  is the decimal equivalent of the 3 bit input.

5(b) For the function  $F(a,b,c,d) = \sum(2,5,11,15)$  and  $X(a,b,c,d) = \sum(1,3,4,6,7,8)$  where  $X(a,b,c,d)$  represents don't-care conditions find

(i) Two level NAND realization by minimizing  $F$  by K Map

(ii) Two level NOR realization by minimizing  $F'$  by K Map and applying De Morgan's theorem on the resulting function

(iii) Three level NOR realization by minimizing  $F$  by K Map, complementing both sides of the resulting function and applying De Morgan's Theorem on R.H.S (you will need an inverter at the third level to get  $F$  from  $F'$ )

(iv) Three level NAND realization by minimizing  $F'$  by K Map, and using an inverter in the third level.

6(a) Implement the following Boolean Functions with an  $8 \times 1$  multiplexer.

$F_1(A,B,C,D) = \sum(0,3,4,6,8,10,12,13,15)$

$F_2(A,B,C,D) = \sum(0,3,5,6,7,10,11,13,14)$

6(b) (i) Design a one-bit comparator circuit using only NAND gates. (ii) Using one-bit magnitude

comparator as the building block construct a 4-bit magnitude comparator. Use NAND gates for interconnection as required.

7(a) Draw the internal diagram of an edge-triggered D flip-flop and explain how edge triggering is achieved in this flip-flop. Also, explain the significance of setup time and hold time.

7(b) Design a mod-9 Binary Counter using 'detect and steer' method. Use JK Flip-flops. Explain how you take care of the unused states in the counter. The counter should be self-correcting

8(a) Draw the schematic diagram of a 4-bit bidirectional shift register with parallel load feature and explain its operation.

8(b) Design a counter with JK flip flops by excitation table method to satisfy the specification when an input 'x' is 0 the counter should cycle through 000->001->010->100->000 and when the input 'x' is 1 the counter should cycle through 000->001->011->111->110->100->000. The counter must be self-correcting.

Educationobserver.com