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2005 NATIONAL INSTITUTE OF TECHNOLOGY

B.TECH DEGREE EXAMINATIONS

PULSE AND DIGITAL CIRCUITS

(EEE)

NOV 2005

TIME:3 HOUR
MARK:70

ANSWER ALL THE QUESTIONS

1) Transistors with Icmax = 200mA and Rbb' = 50 ohms , Cc = 6 pF , CTe = 5 pF , B = 50 , fT = 10 Mhz Ts = 700ns are used to design a collector coupled astable multivibrator operating from 9V supply.

(i)Design the system for 100kHz frequency and 50% duty ratio. Use a base overdrive factor of 5. The design should include the effect of transistor voltages. Use 0.5V, 0.7V and 0.2V for cut-in voltage, base-emitter voltage and saturation voltage respectively. The collector waveforms must have straight edges and the high level output should not go below 8 Volt when a load resistance of 10k is connected at one of the output terminals.

(ii) In the above design the base voltage of the off transistor is expected to start at –8.3V.However it will be found to start at a voltage lower in magnitude. This happens because the transistor which just now went OFF dumped its base stored charge through the timing capacitor into the collector of the companion transistor and in that process reduced the capacitor voltage almost instantaneously even before timing could start. Calculate the stored base charge in the transistor and estimate the new voltage at which capacitor will start timing. And also estimate the actual running frequency. Assume that the load resistance is not connected in solving this part.

(iii) The load resistance of 10k is connected at one collector now. Will the Astable run at design frequency? Will the duty ratio be 50%? If not, calculate the new values accounting for the saturation charge effect described in

2) Design a Astable circuit to run from 12V supply using transistors with following specs - Bmin = 100 , ICmax = 20mA Vebo = 9V.The output should be a square wave of duty ratio 20%.It should have straight edges and the frequency must be 50kHz. You will have to insert a diode in series with emitter line to avoid breakdown of BE junction when a transistor goes off. Account for the forward drop of the diode alongwith base-emitter drop in your design. What will happen if the diodes are not used ? Will the transistors get damaged ? If not , will the Astable continue to function ? If yes, what will be the frequency of operation and duty ratio of operation ?

3) Design a Fixed Bias Transistor Bistable Circuit operating from +5V and –5V DC Supplies using transistors with Bmin = 50 and ICmax = 200mA. The high level output must be around 4.5V and the transistors must operate with a forward overdrive factor of 5 to 7. Assume that the base saturation time constant is 500ns and calculate the saturation charge storage charge in the Base. This charge flowing out through the commutating capacitor must not change its voltage by more than 10%. Design the commutating capacitor value suitably. With the calculated value of commutating capacitance calculate the settling time of the Binary. Use 0.5V, 0.7V and 0.2V for cut-in voltage, base-emitter voltage and saturation voltage respectively.

4) Design a Collector Coupled Monostable Circuit to operate from 12 Volt supply and to generate a 1ms pulse width. Show the trigger circuit design also. The pulse output should have an amplitude > 10 Volt. A load of 4.7k will be connected at the output and this has to be accounted for in the design. Specify all the components. State and justify your assumptions. Does it matter to which collector output the 4.7k load is connected? If it matters, then prepare two designs.

5) Design a collector coupled monostable circuit to produce a pulse of 10V amplitude and 10uS pulse width using a 12V supply voltage. The transistors have the same specifications as in the Problem-1.Estimate the deviation in the pulse width due to the charge loss mechanism described in Problem-1 in your design

6) Find the transfer curve V0 Vs VI .(ii) Find the maximum positive and negative voltages that can be applied at the input without causing saturation in any transistor.(iii) Plot the outputs Vo and V01 when Vi = 5 Sin 314t volts.(iv) Redesign the circuit to get Vut = 2.5V and Vlt = - 2.5V keeping the current in T3 at the same value. Use the ? 10V supply. Plot the outputs Vo and V01 when Vi

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= 5 Sin 314t volts in this case too

7. One input of a standard TTL Nand Gate is held high. The other input is given a 0 to 5V square wave at 1Mhz. The input wave has negligible rise and fall times. The output of this gate is given to the input of another similar gate. Which gate takes higher average supply current? Why? Which gate runs hotter and why?

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