NAME_____ ROLLNO_____

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY-2008

II B.TECH SUPPLIMENTARY EXAMINATIONS
PULSE AND DIGITAL CIRCUITS
(BIO-MEDICAL ENGINEERING)

AUG/SEP-2008

MARK-3 HOUR
MARK-80

ANSWER ANY FIVE QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.
MARKS [16*5=80]

1. (a) A symmetrical square wave is applied to a HP circuit having R = 20 k and C = 0.05 μ f. If the frequency of input signal is 1kHz and the signal swings ±0.5V, draw the output wave shape and indicate the voltages.

(b) What happens if the signal frequency of the signal is reduced to 100 Hz? Show output curve.

2. (a) Explain the response of the clamping circuit when a square wave input is applied under steady state conditions.

(b) Explain the effect of diode characteristics on clamping voltage.

3. Write Short notes on:

(a) Diode switching times

(b) Switching characteristics of transistors

(c) FET as a switch.

4. (a) What are the different types of multivibrators? Name them and sketch their circuits.

(b) Design an astable multi for an o/p amplitude of 15V and square wave frequency of 500Hz. Assume hFEmin = 50, ICsat = 5mA and VCEsat = 0.

5. (a) With the help of a neat circuit diagram and waveforms explain the working of a transistor Miller time base generator.

(b) Find the component values of a bootstrap sweep generator, given Vcc=18V, Ic(sat) = 2mA and hfe(min)=30.

6. (a) Explain the factors which influence the stability of a relaxation divider with the help of a neat waveforms.

(b) A UJT sweep operates with Vv = 3V, Vp=16V and ?=0.5. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1kHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronism with the sync signal?

7. (a) What is sampling gate? Explain how it differ from Logic gates?

(b) What is pedestal? How it effects the output of a sampling gates?

(c) What are the drawbacks of two diode sampling gate?

8. (a) Why totem pole is used in DTL? Draw the circuit diagram and explain a DTL gate with this.

(b) Verify the truth table of RTL NOR gate with the circuit diagram of two inputs.