NAME_____ ROLLNO_____

2007–ANNA UNIVERSITY

B.E/B.TECH DEGREE EXAMINATION

DIGITAL ELECTRONICS

(ELECTRONICS AND COMMUNICATION ENGINEERING)

JUNE-2007

TIME-3 HOUR
MARKS-100

ANSWER ALL QUESTIONS.

PART A - (10 * 2 = 20 MARKS)

1. State and prove Demorgan's theorem.

2. What do you mean by the gray code? What are its applications.

3. What is Demultiplexer.

4. What is Tristate Gate.

5. What is flip-flop also known as a latch?

6. What is a sysnchronous sequential circuit/

7. Difference between Moore and Mealy circuit.

8. What is transition Table.

9. Comparison between PAL and PLA.

10. What is FBGA. Explain it briefly.

PART B - (5 * 16 = 80 MARKS)

11.a. Simply the four variable switching function F(A,B.C.D) = em(3,5,6,8,9,12,13,14)+ ed(0,2,7).

OR

b. Prove that
a) If A + B = A + C and A' + B = A' + C , then B = C.
b) If A + B = A + C and AB = AC, then B = C.
c) Given AB' + A'B = C, show that AC' + A'C = B.

12.a. Realize F(W,X,Y,Z) = S(1,4,6,7,8,9,10,11,15) using 4- to -1 Mux.

OR

b. Design a Binary to Gray converter?

13.a. Draw the circuit and explain the working operation of JKMS flip-flop.

OR

b. Explain the various steps in the analysis of synchronous sequential circuits with suitable example.

14.a. Implement the switching function f(x1 x2 x3) = x1 x2' + x2 x3 by a static hazard free 2 level AND-OR gate network.

OR

b.i)What is the characteristic equation of a D flip-flop?

ii)Using JK flip-flops,design a parallel counter which counts in the sequence 101,110,001,010,000,111,101,.....

15.a.Implement binary to excess 3 code converter using ROM.

OR

b. Design a PLA circuit for F1 = Sm(2,4,7), F2 = Sm(1,6,7)

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