

2007-ANNA UNIVERSITY
B.E/B.TECH DEGREE EXAMINATION
COMPUTER ARCHITECTURE
(ELECTRONICS AND COMMUNICATION ENGINEERING)

JUNE-2007

TIME-3 HOUR
MARKS-100

ANSWER ALL QUESTIONS.

PART A - (10 * 2 = 20 MARKS)

1. Registers R1 and R2 of a computer contain the decimal values 1200 and 4600. What is the effective address of the memory operand in each of the following instructions?
(a) Load 20(R1), R5
(b) Add - (R2), R5.
2. What is the use of Condition Code register?
3. What do you mean by End—around carry correction?
4. Discuss the role of Booth algorithm in the design of Fast Multipliers.
5. Why is the Wait—for—Memory-Function-Completed step needed when reading from or writing to the main memory?
6. Write the sequence of control steps required for three bus structure for the following instruction:
1. Add R4, R5 and R6.
7. Define Locality of Reference.
8. Give the features of a ROM cell.
9. What is the difference between a Subroutine and an Interrupt — service routine?
10. Define Bus Arbitration.

PART B - (5 * 16 = 80 MARKS)

11. (a) Explain in detail the different Instruction types and Instruction Sequencing.
Or
(b) Explain the different types of Addressing modes with suitable examples.
12. (a) Illustrate Booth Algorithm with an example.
Or
(b) Design a 4-bit Carry-Lookahead Adder.
13. (a) Write a Microroutine for the instruction, Add (Rsrc) + Rdst where the source and destination operands are specified in indexed and register addressing modes, respectively.
Or
(b) Explain Microprogrammed Control Unit. What are the advantages and disadvantages of it?
14. (a) Define Cache Mapping Functions. Explain the methods.
Or
(b) How a virtual address gets translated into a physical address? Explain in detail with a neat diagram. Explain the use of TLB.
15. (a) Explain the use of DMA Controllers in a computer system with a neat diagram.
Or
(b) Explain Handshake protocol. Depict clearly how it controls data transfer during an input operation.