UNIT 3
Electronics Devices

2011 **ONE MARK**

MCQ 3.1

Drift current in the semiconductors depends upon

(A) only the electric field

(B) only the carrier concentration gradient

(C) both the electric field and the carrier concentration

(D) both the electric field and the carrier concentration gradient

MCQ 3.2

A Zener diode, when used in voltage stabilization circuits, is biased in

(A) reverse bias region below the breakdown voltage

(B) reverse breakdown region

(C) forward bias region

(D) forward bias constant current mode

MCQ 3.3

A silicon PN junction is forward biased with a constant current at room temperature. When the temperature is increased by 10°C, the forward bias voltage across the PN junction

(A) increases by 60 mV

(B) decreases by 60 mV

(C) increases by 25 mV

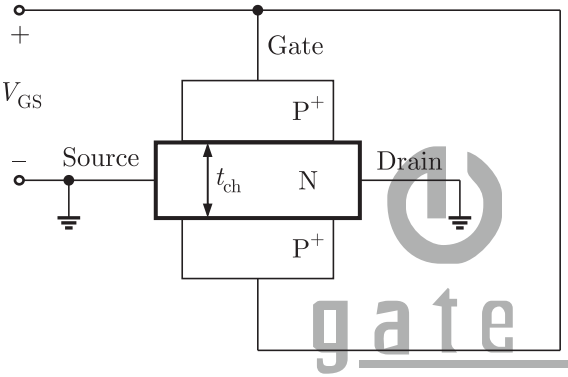
(D) decreases by 25 mV

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

2011 **TWO MARKS**

Common Data Questions: 3.4 & 3.5 :

The channel resistance of an N-channel JFET shown in the figure below is 600 Ω when the full channel thickness (t_{ch}) of 10 μm is available for conduction. The built-in voltage of the gate P^+N junction (V_{bi}) is −1 V. When the gate to source voltage (V_{GS}) is 0 V, the channel is depleted by 1 μm on each side due to the built in voltage and hence the thickness available for conduction is only 8 μm



MCQ 3.4

The channel resistance when $V_{GS} = -3$ V is

(A) 360 Ω (B) 917 Ω

(C) 1000 Ω (D) 3000 Ω

MCQ 3.5

The channel resistance when $V_{GS} = 0$ V is

(A) 480 Ω (B) 600 Ω

(C) 750 Ω (D) 1000 Ω

2010 **ONE MARK**

MCQ 3.6

At room temperature, a possible value for the mobility of electrons in the inversion layer of a silicon n-channel MOSFET is

(A) 450 cm^2/V-s (B) 1350 cm^2/V-s

(C) 1800 cm^2/V-s (D) 3600 cm^2/V-s

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

MCQ 3.7

Thin gate oxide in a CMOS process in preferably grown using

(A) wet oxidation (B) dry oxidation

(C) epitaxial oxidation (D) ion implantation

2010 TWO MARKS

MCQ 3.8

In a uniformly doped BJT, assume that N_E, N_B and N_C are the emitter, base and collector doping in atoms/cm^3, respectively. If the emitter injection efficiency of the BJT is close unity, which one of the following condition is TRUE

(A) $N_E = N_B = N_C$ (B) $N_E >> N_B$ and $N_B > N_C$

(C) $N_E = N_B$ and $N_B < N_C$ (D) $N_E < N_B < N_C$

MCQ 3.9

Compared to a p-n junction with $N_A = N_D = 10^{14}/\text{cm}^3$, which one of the following statements is TRUE for a p-n junction with $N_A = N_D = 10^{20}/\text{cm}^3$?

(A) Reverse breakdown voltage is lower and depletion capacitance is lower

(B) Reverse breakdown voltage is higher and depletion capacitance is lower

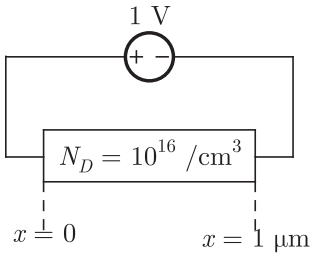
(C) Reverse breakdown voltage is lower and depletion capacitance is higher

(D) Reverse breakdown voltage is higher and depletion capacitance is higher

Statements for Linked Answer Question : 3.10 & 3.11 :

The silicon sample with unit cross-sectional area shown below is in thermal equilibrium. The following information is given: $T = 300\,\text{K}$ electronic charge $= 1.6 \times 10^{-19}\,\text{C}$, thermal voltage $= 26\,\text{mV}$ and electron mobility $= 1350\,\text{cm}^2/\text{V-s}$

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in



MCQ 3.10

The magnitude of the electric field at $x = 0.5\,\mu m$ is

(A) 1 kV/cm (B) 5 kV/cm

(C) 10 kV/cm (D) 26 kV/cm

MCQ 3.11

The magnitude of the electron of the electron drift current density at $x = 0.5\,\mu m$ is

(A) 2.16×10^4 A/cm^2 (B) 1.08×10^4 A/m^2

(C) 4.32×10^3 A/cm^2 (D) 6.48×10^2 A/cm^2

2009 ONE MARK

MCQ 3.12

In an n-type silicon crystal at room temperature, which of the following can have a concentration of 4×10^{19} cm^{-3}?

(A) Silicon atoms (B) Holes

(C) Dopant atoms (D) Valence electrons

MCQ 3.13

The ratio of the mobility to the diffusion coefficient in a semiconductor has the units

(A) V^{-1} (B) cm.V^1

(C) V.cm^{-1} (D) $V.s$

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

MCQ 3.14

Consider the following two statements about the internal conditions in a $n-$channel MOSFET operating in the active region.

S1 : The inversion charge decreases from source to drain

S2 : The channel potential increases from source to drain.

Which of the following is correct?

(A) Only S2 is true

(B) Both S1 and S2 are false

(C) Both S1 and S2 are true, but S2 is not a reason for S1

(D) Both S1 and S2 are true, and S2 is a reason for S1

Common Date for Question 3.13 and 3.14

Consider a silicon $p-n$ junction at room temperature having the following parameters:

Doping on the n-side $= 1\times10^{17}$ cm^{-3}

Depletion width on the n-side $= 0.1\mu m$

Depletion width on the $p-$side $= 1.0\mu m$

Intrinsic carrier concentration $= 1.4\times10^{10}$ cm^{-3}

Thermal voltage $= 26$ mV

Permittivity of free space $= 8.85\times10^{-14}$ F.cm^{-1}

Dielectric constant of silicon $= 12$

MCQ 3.15

The built-in potential of the junction

(A) is 0.70 V

(B) is 0.76 V

(C) is 0.82 V

(D) Cannot be estimated from the data given

MCQ 3.16

The peak electric field in the device is

(A) 0.15 MV . cm^{-1}, directed from $p-$region to $n-$region

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

(B) 0.15 MV . cm^{-1}, directed from n −region to p −region

(C) 1.80 MV . cm^{-1}, directed from p-retion to n −region

(D) 1.80 MV . cm^{-1}, directed from n −region to p −region

2008 **ONE MARK**

MCQ 3.17

Which of the following is NOT associated with a $p - n$ junction ?

(A) Junction Capacitance (B) Charge Storage Capacitance

(C) Depletion Capacitance (D) Channel Length Modulations

MCQ 3.18

Which of the following is true?

(A) A silicon wafer heavily doped with boron is a p^+ substrate

(B) A silicon wafer lightly doped with boron is a p^+ substrate

(C) A silicon wafer heavily doped with arsenic is a p^+ substrate

(D) A silicon wafer lightly doped with arsenic is a p^+ substrate

MCQ 3.19

A silicon wafer has 100 nm of oxide on it and is furnace at a temperature above 1000° C for further oxidation in dry oxygen. The oxidation rate

(A) is independent of current oxide thickness and temperature

(B) is independent of current oxide thickness but depends on temperature

(C) slows down as the oxide grows

(D) is zero as the existing oxide prevents further oxidation

MCQ 3.20

The drain current of MOSFET in saturation is given by $I_D = K(V_{GS} - V_T)^2$ where K is a constant.

The magnitude of the transconductance g_m is

(A) $\dfrac{K(V_{GS} - V_T)^2}{V_{DS}}$ (B) $2K(V_{GS} - V_T)$

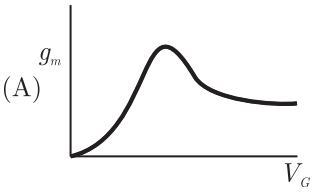
GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

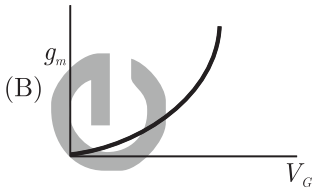
(C) $\frac{I_d}{V_{GS} - V_{DS}}$ (D) $\frac{K(V_{GS} - V_T)^2}{V_{GS}}$

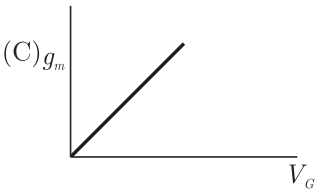
2008 TWO MARKS

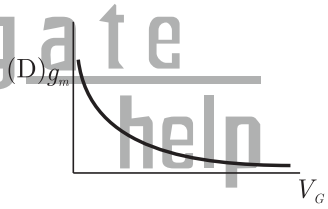
MCQ 3.21

The measured trans conductance g_m of an NMOS transistor operating in the linear region is plotted against the gate voltage V_G at a constant drain voltage V_D. Which of the following figures represents the expected dependence of g_m on V_G ?

(A) 

(B) 

(C) 

(D) 

MCQ 3.22

Silicon is doped with boron to a concentration of 4×10^{17} atoms cm^3 . Assume the intrinsic carrier concentration of silicon to be 1.5×10^{10} / cm^3 and the value of kT/q to be 25 mV at 300 K. Compared to undopped silicon, the fermi level of doped silicon

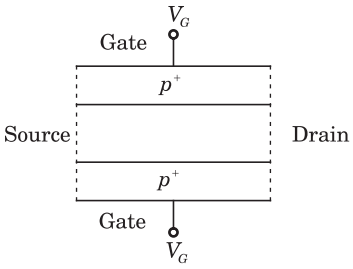
(A) goes down by 0.31 eV (B) goes up by 0.13 eV

(C) goes down by 0.427 eV (D) goes up by 0.427 eV

MCQ 3.23

The cross section of a JFET is shown in the following figure. Let V_c be -2 V and let V_P be the initial pinch -off voltage. If the width W is doubled (with other geometrical parameters and doping levels remaining the same), then the ratio between the mutual trans conductances of the initial and the modified JFET is

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY ISBN: 9788192276236
Visit us at: www.nodia.co.in



(A) 4

(B) $\frac{1}{2}\left(\frac{1-\sqrt{2/V_p}}{1-\sqrt{1/2\,V_p}}\right)$

(C) $\left(\frac{1-\sqrt{2/V_p}}{1-\sqrt{1/2\,V_p}}\right)$

(D) $\frac{1-(2-\sqrt{V_p})}{1-[1\,(2\sqrt{V_p})]}$

MCQ 3.24

Consider the following assertions.

S1 : For Zener effect to occur, a very abrupt junction is required.

S2 : For quantum tunneling to occur, a very narrow energy barrier is required.

Which of the following is correct ?

(A) Only S2 is true

(B) S1 and S2 are both true but S2 is not a reason for S1

(C) S1 and S2 and are both true but S2 is not a reason for S1

(D) Both S1 and S2 are false

2007 **ONE MARK**

MCQ 3.25

The electron and hole concentrations in an intrinsic semiconductor are n_i per cm^3 at 300 K. Now, if acceptor impurities are introduced with a concentration of N_A per cm^3 (where $N_A >> n_i$, the electron concentration per cm^3 at 300 K will be)

(A) n_i

(B) $n_i + N_A$

(C) $N_A - n_i$

(D) $\frac{n_i^2}{N_A}$

MCQ 3.26

In a p^+n junction diode under reverse biased the magnitude of electric

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

field is maximum at

(A) the edge of the depletion region on the p-side

(B) the edge of the depletion region on the n-side

(C) the p^+n junction

(D) the centre of the depletion region on the n-side

2007 **TWO MARKS**

MCQ 3.27

Group I lists four types of $p-n$ junction diodes. Match each device in Group I with one of the option in Group II to indicate the bias condition of the device in its normal mode of operation.

Group - I	Group-II
(P) Zener Diode	(1) Forward bias
(Q) Solar cell	(2) Reverse bias
(R) LASER diode	
(S) Avalanche Photodiode	

(A) P - 1, Q - 2, R - 1, S - 2

(B) P - 2, Q - 1, R - 1, S - 2

(C) P - 2, Q - 2, R - 1, S- -2

(D) P - 2, Q - 1, R - 2, S - 2

MCQ 3.28

Group I lists four different semiconductor devices. match each device in Group I with its characteristic property in Group II

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

Group-I	Group-II
(P) BJT	(1) Population iniversion
(Q) MOS capacitor	(2) Pinch-off voltage
(R) LASER diode	(3) Early effect
(S) JFET	(4) Flat-band voltage

(A) P - 3, Q - 1, R - 4, S - 2

(B) P - 1, Q - 4, R - 3, S - 2

(C) P - 3, Q - 4, R - 1, S - 2

(D) P - 3, Q - 2, R - 1, S - 4

MCQ 3.29

A p^+n junction has a built-in potential of 0.8 V. The depletion layer width a reverse bias of 1.2 V is 2 μm. For a reverse bias of 7.2 V, the depletion layer width will be

(A) 4 μm (B) 4.9 μm

(C) 8 μm (D) 12 μm

MCQ 3.30

The DC current gain (β) of a BJT is 50. Assuming that the emitter injection efficiency is 0.995, the base transport factor is

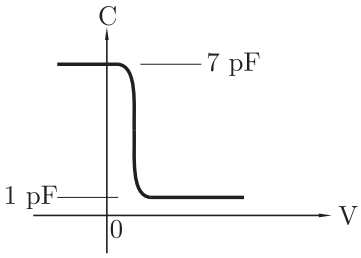
(A) 0.980 (B) 0.985

(C) 0.990 (D) 0.995

Common Data Question 2.29, 2.30 and 2.31 :

The figure shows the high-frequency capacitance - voltage characteristics of Metal/Sio²/silicon (MOS) capacitor having an area of 1×10^{-4} cm². Assume that the permittivities ($\varepsilon_0 \varepsilon_r$) of silicon and Sio_2 are 1×10^{-12} F/cm and 3.5×10^{-13} F/cm respectively.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY ISBN: 9788192276236
Visit us at: www.nodia.co.in



MCQ 3.31

The gate oxide thickness in the MOS capacitor is

(A) 50 nm (B) 143 nm

(C) 350 nm (D) 1 μm

MCQ 3.32

The maximum depletion layer width in silicon is

(A) 0.143 μm (B) 0.857 μm

(C) 1 μm (D) 1.143 μm

MCQ 3.33

Consider the following statements about the $C-V$ characteristics plot :

S1 : The MOS capacitor has as n-type substrate

S2 : If positive charges are introduced in the oxide, the $C-V$ polt will shift to the left.

Then which of the following is true?

(A) Both S1 and S2 are true

(B) S1 is true and S2 is false

(C) S1 is false and S2 is true

(D) Both S1 and S2 are false

2006 ONE MARK

MCQ 3.34

The values of voltage (V_D) across a tunnel-diode corresponding to peak and valley currents are V_p, V_D respectively. The range of tunnel-diode voltage for V_D which the slope of its $I-V_D$ characteristics is

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY ISBN: 9788192276236
Visit us at: www.nodia.co.in

negative would be

(A) $V_D < 0$ (B) $0 \leq V_D < V_p$

(C) $V_p \leq V_D < V_v$ (D) $V_D \geq V_v$

MCQ 3.35

The concentration of minority carriers in an extrinsic semiconductor under equilibrium is

(A) Directly proportional to doping concentration

(B) Inversely proportional to the doping concentration

(C) Directly proportional to the intrinsic concentration

(D) Inversely proportional to the intrinsic concentration

MCQ 3.36

Under low level injection assumption, the injected minority carrier current for an extrinsic semiconductor is essentially the

(A) Diffusion current (B) Drift current

(C) Recombination current (D) Induced current

MCQ 3.37

The phenomenon known as "Early Effect" in a bipolar transistor refers to a reduction of the effective base-width caused by

(A) Electron - hole recombination at the base

(B) The reverse biasing of the base - collector junction

(C) The forward biasing of emitter-base junction

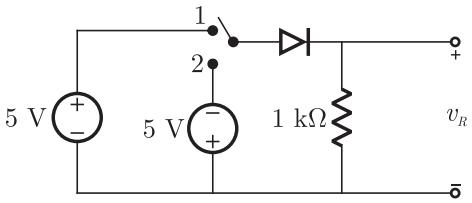
(D) The early removal of stored base charge during saturation-to-cut off switching

2006 TWO MARKS

MCQ 3.38

In the circuit shown below, the switch was connected to position 1 at $t < 0$ and at $t = 0$, it is changed to position 2. Assume that the diode has zero voltage drop and a storage time t_s. For $0 < t \leq t_s$, v_R is given by (all in Volts)

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY ISBN: 9788192276236
Visit us at: www.nodia.co.in



(A) $v_R = -5$ (B) $v_R = +5$

(C) $0 \le v_R < 5$ (D) $-5 \le v_R < 0$

MCQ 3.39

The majority carriers in an n-type semiconductor have an average drift velocity v in a direction perpendicular to a uniform magnetic field B. The electric field E induced due to Hall effect acts in the direction

(A) $v \times B$ (B) $B \times v$

(C) along v (D) opposite to v

MCQ 3.40

Find the correct match between Group 1 and Group 2

Group 1	Group 2
E - Varactor diode	1. Voltage reference
F - PIN diode	2. High frequency switch
G - Zener diode	3. Tuned circuits
H - Schottky diode	4. Current controlled attenuator

(A) E - 4, F - 2, G - 1, H - 3

(B) E - 3, F - 4, G - 1, H - 3

(C) E - 2, F - 4, G - 1, H - 2

(D) E - 1, F - 3, G - 2, H - 4

MCQ 3.41

A heavily doped n- type semiconductor has the following data:

Hole-electron ratio : 0.4

Doping concentration : 4.2×10^8 atoms/m^3

Intrinsic concentration : 1.5×10^4 atoms/m^3

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

The ratio of conductance of the $n-$type semiconductor to that of the intrinsic semiconductor of same material and ate same temperature is given by

(A) 0.00005 (B) 2000

(C) 10000 (D) 20000

2005 **ONE MARK**

MCQ 3.42

The bandgap of Silicon at room temperature is

(A) 1.3 eV (B) 0.7 eV

(C) 1.1 eV (D) 1.4 eV

MCQ 3.43

A Silicon PN junction at a temperature of 20° C has a reverse saturation current of 10 pico - Ameres (pA). The reserve saturation current at 40°C for the same bias is approximately

(A) 30 pA (B) 40 pA

(C) 50 pA (D) 60 pA

MCQ 3.44

The primary reason for the widespread use of Silicon in semiconductor device technology is

(A) abundance of Silicon on the surface of the Earth.

(B) larger bandgap of Silicon in comparison to Germanium.

(C) favorable properties of Silicon - dioxide (SiO_2)

(D) lower melting point

2005 **TWO MARKS**

MCQ 3.45

A Silicon sample A is doped with 10^{18} atoms/cm^3 of boron. Another sample B of identical dimension is doped with 10^{18} atoms/cm^3 phosphorus. The ratio of electron to hole mobility is 3. The ratio of conductivity of the sample A to B is

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY ISBN: 9788192276236
Visit us at: www.nodia.co.in

(A) 3 (B) $\frac{1}{3}$

(C) $\frac{2}{3}$ (D) $\frac{3}{2}$

MCQ 3.46

A Silicon PN junction diode under reverse bias has depletion region of width 10 μm. The relative permittivity of Silicon, $\varepsilon_r = 11.7$ and the permittivity of free space $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m. The depletion capacitance of the diode per square meter is

(A) 100 μF (B) 10 μF

(C) 1 μF (D) 20 μF

MCQ 3.47

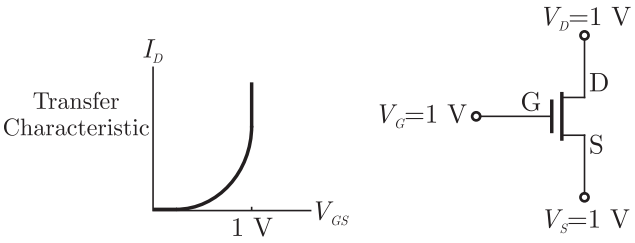
A MOS capacitor made using p type substrate is in the accumulation mode. The dominant charge in the channel is due to the presence of

(A) holes (B) electrons

(C) positively charged icons (D) negatively charged ions

MCQ 3.48

For an n-channel MOSFET and its transfer curve shown in the figure, the threshold voltage is



(A) 1 V and the device is in active region

(B) −1 V and the device is in saturation region

(C) 1 V and the device is in saturation region

(D) −1 V and the device is an active region

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

MCQ 3.49

The impurity commonly used for realizing the base region of a silicon $n-p-n$ transistor is

(A) Gallium (B) Indium

(C) Boron (D) Phosphorus

MCQ 3.50

If for a silicon npn transistor, the base-to-emitter voltage (V_{BE}) is 0.7 V and the collector-to-base voltage (V_{CB}) is 0.2 V, then the transistor is operating in the

(A) normal active mode (B) saturation mode

(C) inverse active mode (D) cutoff mode

MCQ 3.51

Consider the following statements S1 and S2.

S1 : The β of a bipolar transistor reduces if the base width is increased.

S2 : The β of a bipolar transistor increases if the dopoing concentration in the base is increased.

Which remarks of the following is correct ?

(A) S1 is FALSE and S2 is TRUE

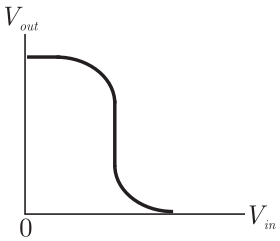
(B) Both S1 and S2 are TRUE

(C) Both S1 and S2 are FALSE

(D) S1 is TRUE and S2 is FALSE

MCQ 3.52

Given figure is the voltage transfer characteristic of



(A) an NOMS inverter with enhancement mode transistor as load

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

(B) an NMOS inverter with depletion mode transistor as load

(C) a CMOS inverter

(D) a BJT inverter

MCQ 3.53

Assuming $V_{CEsat} = 0.2$ V and $\beta = 50$, the minimum base current (I_B) required to drive the transistor in the figure to saturation is

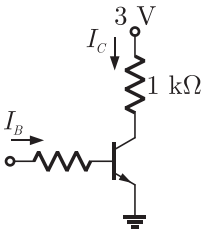


Fig Q.

(A) 56 μA

(B) 140 mA

(C) 60 mA

(D) 3 mA

2004 **TWO MARKS**

MCQ 3.54

In an abrupt $p-n$ junction, the doping concentrations on the p −side and n-side are $N_A = 9\times10^{16}$ /cm^3 respectively. The $p-n$ junction is reverse biased and the total depletion width is 3 μm. The depletion width on the p −side is

(A) 2.7 μm

(B) 0.3 μm

(C) 2.25 μm

(D) 0.75 μm

MCQ 3.55

The resistivity of a uniformly doped n −type silicon sample is 0.5Ω - mc. If the electron mobility (μ_n) is 1250 cm^2/V-sec and the charge of an electron is 1.6×10^{-19} Coulomb, the donor impurity concentration (N_D) in the sample is

(A) 2×10^{16}/cm^3

(B) 1×10^{16}/cm^3

(C) 2.5×10^{15}/cm^3

(D) 5×10^{15}/cm^3

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

MCQ 3.56

Consider an abrupt $p-n$ junction. Let V_{bi} be the built-in potential of this junction and V_R be the applied reverse bias. If the junction capacitance (C_j) is 1 pF for $V_{bi}+V_R=1$ V, then for $V_{bi}+V_R=4$ V, C_j will be

(A) 4 pF
(B) 2 pF
(C) 0.25 pF
(D) 0.5 pF

MCQ 3.57

Consider the following statements Sq and S2.

S1 : The threshold voltage (V_T) of MOS capacitor decreases with increase in gate oxide thickness.

S2 : The threshold voltage (V_T) of a MOS capacitor decreases with increase in substrate doping concentration.

Which Marks of the following is correct ?

(A) S1 is FALSE and S2 is TRUE
(B) Both S1 and S2 are TRUE
(C) Both S1 and S2 are FALSE
(D) S1 is TRUE and S2 is FALSE

MCQ 3.58

The drain of an n-channel MOSFET is shorted to the gate so that $V_{GS}=V_{DS}$. The threshold voltage (V_T) of the MOSFET is 1 V. If the drain current (I_D) is 1 mA for $V_{GS}=2$ V, then for $V_{GS}=3$ V, I_D is

(A) 2 mA
(B) 3 mA
(C) 9 mA
(D) 4 mA

MCQ 3.59

The longest wavelength that can be absorbed by silicon, which has the bandgap of 1.12 eV, is 1.1 μm. If the longest wavelength that can be absorbed by another material is 0.87 μm, then bandgap of this material is

(A) 1.416 A/cm^2
(B) 0.886 eV
(C) 0.854 eV
(D) 0.706 eV

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

MCQ 3.60

The neutral base width of a bipolar transistor, biased in the active region, is 0.5 μm. The maximum electron concentration and the diffusion constant in the base are $10^{14}/\text{cm}^3$ and $D_n = 25$ cm^2/sec respectively. Assuming negligible recombination in the base, the collector current density is (the electron charge is 1.6×10^{-19} Coulomb)

(A) 800 A/cm^2 (B) 8 A/cm^2

(C) 200 A/cm^2 (D) 2 A/cm^2

2003 ONE MARK

MCQ 3.61

n-type silicon is obtained by doping silicon with

(A) Germanium (B) Aluminium

(C) Boron (D) Phosphorus

MCQ 3.62

The Bandgap of silicon at 300 K is

(A) 1.36 eV (B) 1.10 eV

(C) 0.80 eV (D) 0.67 eV

MCQ 3.63

The intrinsic carrier concentration of silicon sample at 300 K is 1.5×10^{16} /m^3. If after doping, the number of majority carriers is $5 \times 10^{20}/\text{m}^3$, the minority carrier density is

(A) $4.50 \times 10^{11}/\text{m}^3$ (B) $3.333 \times 10^{4}/\text{m}^3$

(C) $5.00 \times 10^{20}/\text{m}^3$ (D) $3.00 \times 10^{-5}/\text{m}^3$

MCQ 3.64

Choose proper substitutes for X and Y to make the following statement correct Tunnel diode and Avalanche photo diode are operated in X bias ad Y bias respectively

(A) X: reverse, Y: reverse (B) X: reverse, Y: forward

(C) X: forward, Y: reverse (D) X: forward, Y: forward

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

MCQ 3.65

For an $n-$ channel enhancement type MOSFET, if the source is connected at a higher potential than that of the bulk (i.e. $V_{SB} > 0$), the threshold voltage V_T of the MOSFET will

(A) remain unchanged (B) decrease

(C) change polarity (D) increase

2003 TWO MARKS

MCQ 3.66

An $n-$type silicon bar 0.1 cm long and 100 μm^2 i cross-sectional area has a majority carrier concentration of $5\times10^{20}/m^2$ and the carrier mobility is 0.13 m^2/V-s at 300 K. If the charge of an electron is 1.5×10^{-19} coulomb, then the resistance of the bar is

(A) 10^6 Ohm (B) 10^4 Ohm

(C) 10^{-1} Ohm (D) 10^{-4} Ohm

MCQ 3.67

The electron concentration in a sample of uniformly doped n-type silicon at 300 K varies linearly from $10^{17}/cm^3$ at $x = 0$ to $6\times10^{16}/cm^3$ at $x = 2\mu m$. Assume a situation that electrons are supplied to keep this concentration gradient constant with time. If electronic charge is 1.6×10^{-19} coulomb and the diffusion constant $D_n = 35$ cm^2/s, the current density in the silicon, if no electric field is present, is

(A) zero (B) -112 A/cm^2

(C) +1120 A/cm^2 (D) -1120 A/cm^2

MCQ 3.68

Match items in Group 1 with items in Group 2, most suitably.

Group 1	Group 2
P. LED	1. Heavy doping
Q. Avalanche photo diode	2. Coherent radiation
R. Tunnel diode	3. Spontaneous emission
S. LASER	4. Current gain

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

(A) P - 1, Q - 2, R - 4, S - 3

(B) P - 2, Q - 3, R - 1, S - 4

(C) P - 3 Q - 4, R - 1, S - 2

(D) P - 2, Q - 1, R - 4, S - 3

MCQ 3.69

At 300 K, for a diode current of 1 mA, a certain germanium diode requires a forward bias of 0.1435 V, whereas a certain silicon diode requires a forward bias of 0.718 V. Under the conditions state above, the closest approximation of the ratio of reverse saturation current in germanium diode to that in silicon diode is

(A) 1 (B) 5

(C) 4×10^{3} (D) 8×10^{3}

MCQ 3.70

A particular green LED emits light of wavelength 5490 A°. The energy bandgap of the semiconductor material used there is

(Plank's constant $= 6.626\times10^{-34} J-s$)

(A) 2.26 eV (B) 1.98 eV

(C) 1.17 eV (D) 0.74 eV

MCQ 3.71

When the gate-to-source voltage (V_{Gs}) of a MOSFET with threshold voltage of 400 mV, working in saturation is 900 mV, the drain current is observed to be 1 mA. Neglecting the channel width modulation effect and assuming that the MOSFET is operating at saturation, the drain current for an applied V_{GS} of 1400 mV is

(A) 0.5 mA (B) 2.0 mA

(C) 3.5 mA (D) 4.0 mA

MCQ 3.72

If P is Passivation, Q is $n-$well implant, R is metallization and S is source/drain diffusion, then the order in which they are carried out in a standard $n-$well CMOS fabrication process, is

(A) $P-Q-R-S$ (B) $Q-S-R-P$

(C) $R-P-S-Q$ (D) $S-R-Q-P$

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

MCQ 3.73

The action of JFET in its equivalent circuit can best be represented as a

(A) Current controlled current source

(B) Current controlled voltage source

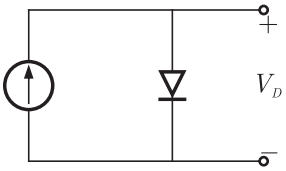
(C) Voltage controlled voltage source

(D) Voltage controlled current source

2002 **ONE MARK**

MCQ 3.74

In the figure, silicon diode is carrying a constant current of 1 mA. When the temperature of the diode is 20°C, V_D is found to be 700 mV. If the temperature rises to 40°C, V_D becomes approximately equal to



(A) 740 mV

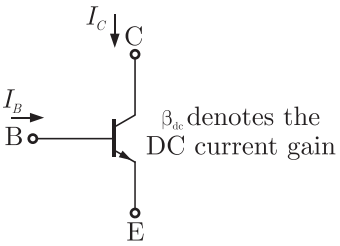
(B) 660 mV

(C) 680 mV

(D) 700 mV

MCQ 3.75

If the transistor in the figure is in saturation, then



(A) I_C is always equal to $\beta_{dc} I_B$

(B) I_C is always equal to $-\beta_{de} I_B$

(C) I_C is greater than or equal to $\beta_{dc} I_B$

(D) I_C is less than or equal to $\beta_{dc} I_B$

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

2001 **ONE MARK**

MCQ 3.76

MOSFET can be used as a

(A) current controlled capacitor (B) voltage controlled capacitor

(C) current controlled inductor (D) voltage controlled inductor

MCQ 3.77

The effective channel length of MOSFET in saturation decreases with increase in

(A) gate voltage (B) drain voltage

(C) source voltage (D) body voltage

1999 **ONE MARK**

MCQ 3.78

The early effect in a bipolar junction transistor is caused by

(A) fast turn-on

(B) fast turn-off

(C) large collector-base reverse bias

(D) large emitter-base forward bias

1999 **TWO MARKS**

MCQ 3.79

An n-channel JEFT has $I_{DSS} = 2\,\text{mA}$ and $V_p = -4\,\text{V}$. Its transconductance g_m (in milliohm) for an applied gate-to-source voltage V_{GS} of $-2\,\text{V}$ is

(A) 0.25 (B) 0.5

(C) 0.75 (D) 1.0

MCQ 3.80

An npn transistor (with $C = 0.3\,\text{pF}$) has a unity-gain cutoff frequency f_T of 400 MHz at a dc bias current $I_c = 1\,\text{mA}$. The value of its C_μ(in pF) is approximately ($V_T = 26\,\text{mV}$)

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

(A) 15 (B) 30
(C) 50 (D) 96

1998 ONE MARK

MCQ 3.81

The electron and hole concentrations in a intrinsic semiconductor are n_i and p_i respectively. When doped with a p-type material, these change to n and p, respectively, Then

(A) $n + p = n_i + p_i$ (B) $n + ni = p + p_i$
(C) $np_i = n_i p$ (D) $np = n_i p_i$

MCQ 3.82

The f_T of a BJT is related to its g_m, C_π and C_μ as follows

(A) $f_T = \dfrac{C_\pi + C_\mu}{g_m}$ (B) $f_T = \dfrac{2\pi(C_\pi + C_\mu)}{g_m}$

(C) $f_T = \dfrac{g_m}{C_\pi + C_\mu}$ (D) $f_T = \dfrac{g_m}{2\pi(C_\pi + C_\mu)}$

MCQ 3.83

The static characteristic of an adequately forward biased p-n junction is a straight line, if the plot is of

(A) $\log I$ vs $\log V$ (B) $\log I$ vs V
(C) I vs $\log V$ (D) I vs V

MCQ 3.84

A long specimen of p-type semiconductor material

(A) is positively charged
(B) is electrically neutral
(C) has an electric field directed along its length
(D) acts as a dipole

MCQ 3.85

Two identical FETs, each characterized by the parameters g_m and r_d are connected in parallel. The composite FET is then characterized by the parameters

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

(A) $\frac{g_m}{2}$ and $2r_d$ (B) $\frac{g_m}{2}$ and $\frac{r_d}{2}$

(C) $2g_m$ and $\frac{r_d}{2}$ (D) $2g_m$ and $2r_d$

MCQ 3.86

The units of $\frac{q}{kT}$ are

(A) V (B) V^{-1}

(C) J (D) J/K

1997 ONE MARK

MCQ 3.87

For a MOS capacitor fabricated on a p-type semiconductor, strong inversion occurs when

(A) surface potential is equal to Fermi potential

(B) surface potential is zero

(C) surface potential is negative and equal to Fermi potential in magnitude

(D) surface potential is positive and equal to twice the Fermi potential

MCQ 3.88

The intrinsic carrier density at 300 K is $1.5 \times 10^{10}/\text{cm}^3$, in silicon. For n-type silicon doped to 2.25×10^{15} atoms/cm^3, the equilibrium electron and hole densities are

(A) $n = 1.5 \times 10^{15}/\text{cm}^3, p = 1.5 \times 10^{10}/\text{cm}^3$

(B) $n = 1.5 \times 10^{10}/\text{cm}^3, p = 2.25 \times 10^{15}/\text{cm}^3$

(C) $n = 2.25 \times 10^{15}/\text{cm}^3, p = 1.0 \times 10^{15}/\text{cm}^3$

(D) $n = 1.5 \times 10^{10}/\text{cm}^3, p = 1.5 \times 10^{10}/\text{cm}^3$

1996 ONE MARK

MCQ 3.89

The p-type substrate in a conventional pn-junction isolated integrated circuit should be connected to

(A) nowhere, i.e. left floating

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

(B) a DC ground potential

(C) the most positive potential available in the circuit

(D) the most negative potential available in the circuit

MCQ 3.90

If a transistor is operating with both of its junctions forward biased, but with the collector base forward bias greater than the emitter base forward bias, then it is operating in the

(A) forward active mode

(B) reverse saturation mode

(C) reverse active mode

(D) forward saturation mode

MCQ 3.91

The common-emitter short-circuit current gain β of a transistor

(A) is a monotonically increasing function of the collector current I_C

(B) is a monotonically decreasing function of I_C

(C) increase with I_C, for low I_C, reaches a maximum and then decreases with further increase in I_C

(D) is not a function of I_C

MCQ 3.92

A n-channel silicon ($E_g = 1.1\,\text{eV}$) MOSFET was fabricated using $n+$ poly-silicon gate and the threshold voltage was found to be 1 V. Now, if the gate is changed to p^+ poly-silicon, other things remaining the same, the new threshold voltage should be

(A) -0.1 V

(B) 0 V

(C) 1.0 V

(D) 2.1 V

1996 TWO MARKS

MCQ 3.93

In a bipolar transistor at room temperature, if the emitter current is doubled the voltage across its base-emitter junction

(A) doubles

(B) halves

(C) increases by about 20 mV

(D) decreases by about 20 mV

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY ISBN: 9788192276236
Visit us at: www.nodia.co.in

MCQ 3.94

An *npn* transistor has a beta cut-off frequency f_β of 1 MHz and common emitter short circuit low-frequency current gain β_o of 200 it unity gain frequency f_T and the alpha cut-off frequency f_α respectively are

(A) 200 MHz, 201 MHz
(B) 200 MHz, 199 MHz
(C) 199 MHz, 200 MHz
(D) 201 MHz, 200 MHz

MCQ 3.95

A silicon n MOSFET has a threshold voltage of 1 V and oxide thickness of Ao.

$[\varepsilon_r(SiO_2) = 3.9, \varepsilon_0 = 8.854 \times 10^{-14}\,F/cm, q = 1.6 \times 10^{-19}\,C]$

The region under the gate is ion implanted for threshold voltage tailoring. The dose and type of the implant (assumed to be a sheet charge at the interface) required to shift the threshold voltage to -1 V are

(A) $1.08 \times 10^{12}/cm^2$, p-type
(B) $1.08 \times 10^{12}/cm^2$, n-type
(C) $5.4 \times 10^{11}/cm^2$, p-type
(D) $5.4 \times 10^{11}/cm^2$, n-type

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

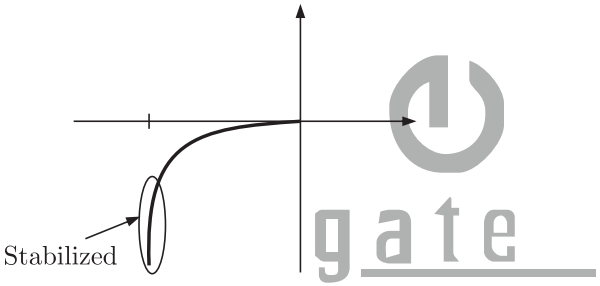
SOLUTIONS

SOL 3.1

Drift current $I_d = qn\mu_n E$
It depends upon Electric field E and carrier concentration n
Hence (C) is correct option.

SOL 3.2

Zener diode operates in reverse breakdown region.



Hence (B) is correct option.

SOL 3.3

For every 1° C increase in temperature, forward bias voltage across diode decreases by 2.5 mV. Thus for 10° C increase, there us 25 mV decreases.
Hence (D) is correct option.

SOL 3.4

Full channel resistance is

$$r\ \frac{\rho \times L}{W \times a} = 600\,\Omega \qquad ...(1)$$

If V_{GS} is applied, Channel resistance is

$$r' = \frac{\rho \times L}{W \times b} \qquad \text{where } b = a\left(1 - \sqrt{\frac{V_{GS}}{V_p}}\right)$$

Pinch off voltage,

$$|V_p| = \frac{qN_D}{2\varepsilon}a^2 \qquad ...(2)$$

If depletion on each side is $d = 1$ μm at $V_{GS} = 0$.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

$$V_j = \frac{qN_D}{2\varepsilon} d^2$$

or $$1 = \frac{qN_D}{2\varepsilon}(1 \times 10^{-6})^2 \Rightarrow \frac{qN_D}{2\varepsilon} = 10^{12}$$

Now from equation (2), we have

$$|V_p| = 10^{12} \times (5 \times 10^{-6})^2$$

or $$V_p = -25\ \text{V}$$

At $V_{GS} = -3\ \text{V}$;

$$b = 5\left(1 - \sqrt{\frac{-3}{-25}}\right)\mu\text{m} = 3.26\,\mu\text{m}$$

$$r' = \frac{\rho L}{W \times b} = \frac{\rho L}{Wa} \times \frac{a}{b} = 600 \times \frac{5}{3.26} = 917\,\Omega$$

Hence (B) is correct option.

SOL 3.5

At $V_{GS} = 0\ \text{V}$, $b = 4\,\mu\text{m}$ since $2b = 8\,\mu\text{m}$

Thus $$r' = \frac{\rho L}{Wa} \times \frac{a}{b} = 600 \times \frac{5}{4} = 750\,\Omega$$

Hence (C) is correct option.

SOL 3.6

At room temperature mobility of electrons for Si sample is given $\mu_n = 1350\ \text{cm}^2/\text{Vs}$. For an n-channel MOSFET to create an inversion layer of electrons, a large positive gate voltage is to be applied. Therefore, induced electric field increases and mobility decreases.
So, Mobility $\mu_n < 1350\ \text{cm}^2/\text{Vs}$ for n-channel MOSFET
Hence (A) is correct option.

SOL 3.7

Dry oxidation is used to achieve high quality oxide growth.
Hence (B) is correct option.

SOL 3.8

Emitter injection efficiency is given as

$$\gamma = \frac{1}{1 + \frac{N_B}{N_E}}$$

To achieve $$\gamma = 1, N_E >> N_B$$

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY ISBN: 9788192276236
Visit us at: www.nodia.co.in

Hence (B) is correct option.

SOL 3.9

Reverse bias breakdown or Zener effect occurs in highly doped PN junction through tunneling mechanism. In a highly doped PN junction, the conduction and valence bands on opposite sides of the junction are sufficiently close during reverse bias that electron may tunnel directly from the valence band on the p-side into the conduction band on n-side.

Breakdown voltage $V_B \propto \dfrac{1}{N_A N_D}$

So, breakdown voltage decreases as concentration increases

Depletion capacitance

$$C = \left\{\frac{e\varepsilon_s N_A N_D}{2(V_{bi} + V_R)(N_A + N_D)}\right\}^{1/2}$$

Thus $C \propto N_A N_D$

Depletion capacitance increases as concentration increases

Hence (C) is correct option.

SOL 3.10

Sample is in thermal equilibrium so, electric field

$$E = \frac{1}{1\,\mu\text{m}} = 10\,\text{kV/cm}$$

Hence (C) is correct option.

SOL 3.11

Electron drift current density

$$\begin{aligned} J_d &= N_D \mu_n e E \\ &= 10^{16} \times 1350 \times 1.6 \times 10^{-19} \times 10 \times 10^{13} \\ &= 2.16 \times 10^4 \text{ A/cm}^2 \end{aligned}$$

Hence (A) is correct option.

SOL 3.12

Only dopant atoms can have concentration of 4×10^{19} cm^{-3} in $n-$ type silicon at room temperature.

Hence option (C) is correct.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

SOL 3.13

Unit of mobility μ_n is $= \dfrac{\text{cm}^2}{V.\text{sec}}$

Unit of diffusion current D_n is $= \dfrac{\text{cm}^2}{\text{sec}}$

Thus unit of $\dfrac{\mu_n}{D_n}$ is $= \dfrac{\text{cm}^2}{V \cdot \text{sec}} / \dfrac{\text{cm}^2}{\text{sec}} = \dfrac{1}{V} = V^{-1}$

Hence option (A) is correct.

SOL 3.14

Both S1 and S2 are true and S2 is a reason for S1.
Hence option (D) is correct.

SOL 3.15

We know that

$$N_A W_P = N_D W_N$$

or $$N_A = \frac{N_D W_N}{W_P} = \frac{1 \times 10^{17} \times 0.1 \times 10^{-6}}{1 \times 10^{-6}} = 1 \times 10^{16}$$

The built-in potential is

$$V_{bi} = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$$= 26 \times 10^{-3} \ln\left(\frac{1 \times 10^{17} \times 1 \times 10^{16}}{(1.4 \times 10^{10})^2}\right) = 0.760$$

Hence option (B) is correct.

SOL 3.16

The peak electric field in device is directed from p to n and is

$$E = -\frac{eN_D x_n}{\varepsilon_s} \quad \text{from } p \text{ to } n$$

$$= \frac{eN_D x_n}{\varepsilon_s} \quad \text{from } n \text{ to } p$$

$$= \frac{1.6 \times 10^{-19} \times 1 \times 10^{17} \times 1 \times 10^{-5}}{8.85 \times 10^{-14} \times 12} = 0.15$$

MV/cm

Hence option (B) is correct.

SOL 3.17

Channel length modulation is not associated with a $p - n$ junction.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

It is being associated with MOSFET in which effective channel length decreases, producing the phenomenon called channel length modulation.
Hence option (D) is correct.

SOL 3.18

Trivalent impurities are used for making $p-$ type semiconductors. So, Silicon wafer heavily doped with boron is a p^+ substrate.
Hence option (A) is correct

SOL 3.19

Oxidation rate is zero because the existing oxide prevent the further oxidation.
Hence option (D) is correct.

SOL 3.20

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}} K(V_{GS} - V_T)^2 = 2K(V_{GS} - V_T)$$

Hence option (B) is correct.

SOL 3.21

As $V_D = \text{constant}$
Thus $g_m \propto (V_{GS} - V_T)$ Which is straight line.
Hence option (C) is correct.

SOL 3.22

$$E_2 - E_1 = kT \ln \frac{N_A}{n_i}$$

$$N_A = 4 \times 10^{17}$$
$$n_i = 1.5 \times 10^{10}$$
$$E_2 - E_1 = 25 \times 10^{-3}\, e \ln \frac{4 \times 10^{17}}{1.5 \times 10^{10}} = 0.427 \text{ eV}$$

Hence fermi level goes down by 0.427 eV as silicon is doped with boron.
Hence option (C) is correct.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

SOL 3.23

Pinch off voltage $V_P = \dfrac{eW^2 N_D}{\varepsilon s}$

Let $V_P = V_{P1}$

Now $\dfrac{V_{P1}}{V_{P2}} = \dfrac{W_1^2}{W_2^2} = \dfrac{W^2}{(2W)^2}$

or $4V_{P1} = V_{P2}$

Initial transconductance

$$g_m = K_n\left[1 - \sqrt{\frac{V_{bi} - V_{GS}}{V_p}}\right]$$

For first condition $g_{m1} = K_n\left[1 - \sqrt{\dfrac{0-(-2)}{V_{P1}}}\right] = K_n\left[1 - \sqrt{\dfrac{2}{V_{P1}}}\right]$

For second condition

$$g_{m2} = K_n\left[1 - \sqrt{\frac{0-(-2)}{V_{P2}}}\right] = K_2\left[1 - \sqrt{\frac{2}{4V_{P1}}}\right]$$

Dividing $\dfrac{g_{m1}}{g_{m2}} = \left(\dfrac{1 - \sqrt{2/V_{P1}}}{1 - \sqrt{1/(2V_{P1})}}\right)$

Hence $V_P = V_{P1}$

Hence option (C) is correct.

SOL 3.24

Hence option (A) is correct.

SOL 3.25

As per mass action law

$$np = n_i^2$$

If acceptor impurities are introduces

$$p = N_A$$

Thus $nN_A = n_i^2$

or $n = \dfrac{n_i^2}{N_A}$

Hence option (D) is correct.

SOL 3.26

The electric field has the maximum value at the junction of $p^+ n$.
Hence option (C) is correct.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

SOL 3.27

Zener diode and Avalanche diode works in the reverse bias and laser diode works in forward bias.
In solar cell diode works in forward bias but photo current is in reverse direction. Thus

Zener diode : Reverse Bias
Solar Cell : Forward Bias
Laser Diode : Forward Bias
Avalanche Photo diode : Reverse Bias

Hence option (B) is correct.

SOL 3.28

In BJT as the B-C reverse bias voltage increases, the B-C space charge region width increases which x_B (i.e. neutral base width) $> A$ change in neutral base width will change the collector current. A reduction in base width will causes the gradient in minority carrier concentration to increase, which in turn causes an increased in the diffusion current. This effect si known as base modulation as early effect.
In JFET the gate to source voltage that must be applied to achieve pinch off voltage is described as pinch off voltage and is also called as turn voltage or threshold voltage.
In LASER population inversion occurs on the condition when concentration of electrons in one energy state is greater than that in lower energy state, i.e. a non equilibrium condition.
In MOS capacitor, flat band voltage is the gate voltage that must be applied to create flat ban condition in which there is no space charge region in semiconductor under oxide.
Therefore

BJT : Early effect
MOS capacitor : Flat-band voltage
LASER diode : Population inversion
JFET : Pinch-off voltage

Hence option (C) is correct.

SOL 3.29

$$W = K\sqrt{V + V_R}$$

Now $$2\mu = K\sqrt{0.8 + 1.2}$$

From above two equation we get

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

$$\frac{W}{2\mu} = \frac{\sqrt{0.8+7.2}}{\sqrt{0.8+1.2}} = \frac{\sqrt{8}}{\sqrt{2}} = 2$$

or $$W_2 = 4\,\mu \text{ m}$$

Hence option (A) is correct.

SOL 3.30

$$\alpha = \frac{\beta}{\beta+1} = \frac{50}{50+1} = \frac{50}{51}$$

Current Gain = Base Transport Factor × Emitter injection Efficiency

$$\alpha = \beta_1 \times \beta_2$$

or $$\beta_1 = \frac{\alpha}{\beta_2} = \frac{50}{51 \times 0.995} = 0.985$$

Hence option (B) is correct.

SOL 3.31

At low voltage when there is no depletion region and capacitance is decide by SiO_2 thickness only.

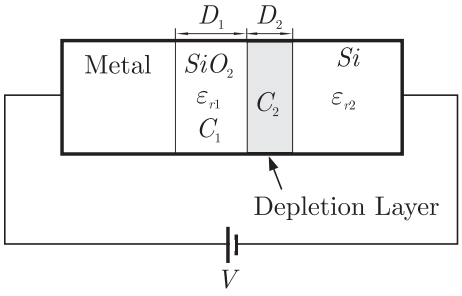
$$C = \frac{\varepsilon_0 \varepsilon_{r1} A}{D}$$

or $$D = \frac{\varepsilon_0 \varepsilon_{r1} A}{C} = \frac{3.5 \times 10^{-13} \times 10^{-4}}{7 \times 10^{-12}} = 50 \text{ nm}$$

Hence option (A) is correct.

SOL 3.32

The construction of given capacitor is shown in fig below



When applied voltage is 0 volts, there will be no depletion region and we get

$$C_1 = 7 \text{ pF}$$

When applied voltage is V, a depletion region will be formed as shown in fig an total capacitance is 1 pF. Thus

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

$$C_T = 1 \text{ pF}$$

or $$C_T = \frac{C_1 C_2}{C_1 + C_2} = 1 \text{ pF}$$

or $$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2}$$

Substituting values of C_T and C_1 we get

$$C_2 = \frac{7}{6} \text{ pF}$$

Now $$D_2 = \frac{\varepsilon_0 \varepsilon_{r2} A}{C_2} = \frac{1 \times 10^{-12} \times 10^{-4}}{\frac{7}{6} \times 10^{-12}} = \frac{6}{7} \times 10^{-4} \text{ cm}$$

$$= 0.857 \ \mu\text{m}$$

Hence option (B) is correct.

SOL 3.33

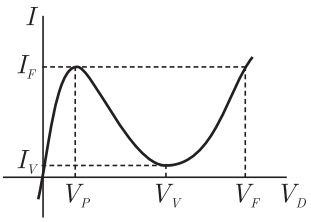
Depletion region will not be formed if the MOS capacitor has n type substrate but from C-V characteristics, C reduces if V is increased. Thus depletion region must be formed. Hence S_1 is false

If positive charges is introduced in the oxide layer, then to equalize the effect the applied voltage V must be reduced. Thus the $C-V$ plot moves to the left. Hence S_2 is true.

Hence option (C) is correct.

SOL 3.34

For the case of negative slope it is the negative resistance region



Hence option (C) is correct.

SOL 3.35

For n-type p is minority carrier concentration

$$np = n_i^2$$

$$np = \text{Constant} \qquad \text{Since } n_i \text{ is constant}$$

$$p \propto \frac{1}{n}$$

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY ISBN: 9788192276236
Visit us at: www.nodia.co.in

Thus p is inversely proportional to n.
Hence option (A) is correct.

SOL 3.36

Diffusion current, since the drift current is negligible for minority carrier.
Hence option (A) is correct.

SOL 3.37

In BJT as the B-C reverse bias voltage increases, the B-C space charge region width increases which x_B (i.e. neutral base width) $> A$ change in neutral base width will change the collector current. A reduction in base width will causes the gradient in minority carrier concentration to increases, which in turn causes an increases in the diffusion current. This effect si known as base modulation as early effect.
Hence option (B) is correct.

SOL 3.38

For $t < 0$ diode forward biased and $V_R = 5$. At $t = 0$ diode abruptly changes to reverse biased and current across resistor must be 0. But in storage time $0 < t < t_s$ diode retain its resistance of forward biased.
Thus for $0 < t < t_s$ it will be ON and

$$V_R = -5 \text{ V}$$

Hence option (A) is correct.

SOL 3.39

According to Hall effect the direction of electric field is same as that of direction of force exerted.

$$E = -v \times B$$

or

$$E = B \times v$$

Hence option (B) is correct.

SOL 3.40

The varacter diode is used in tuned circuit as it can provide frequently stability.
PIN diode is used as a current controlled attenuator.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

Zener diode is used in regulated voltage supply or fixed voltage reference.

Schottkey diode has metal-semiconductor function so it has fast switching action so it is used as high frequency switch

Varactor diode : Tuned circuits

PIN Diode : Current controlled attenuator

Zener diode : Voltage reference

Schottky diode : High frequency switch

Hence option (B) is correct.

SOL 3.41

We have $\dfrac{\mu_P}{\mu_n} = 0.4$

Conductance of n type semiconductor

$$\sigma_n = nq\mu_n$$

Conductance of intrinsic semiconductor

$$\sigma_i = n_i q(\mu_n + \mu_p)$$

Ratio is $\dfrac{\sigma_n}{\sigma_i} = \dfrac{n\mu_n}{n_i(\mu_n + \mu_p)} = \dfrac{n}{n_i\left(1 + \frac{\mu_p}{\mu_n}\right)}$

$$= \frac{4.2 \times 10^8}{1.5 \times 10^4 (1 + 0.4)} = 2 \times 10^4$$

Hence option (D) is correct.

SOL 3.42

For silicon at 0 K,

$$E_{g0} = 1.21 \text{ eV}$$

At any temperature

$$E_{gT} = E_{g0} - 3.6 \times 10^{-4} T$$

At $T = 300$ K,

$$E_{g300} = 1.21 - 3.6 \times 10^{-4} \times 300 = 1.1 \text{ eV}$$

This is standard value, that must be remembered.

Hence option (C) is correct.

SOL 3.43

The reverse saturation current doubles for every $10^\circ C$ rise in temperature as follows :

$$I_0(T) = I_{01} \times 2^{(T - T_1)/10}$$

Thus at 40° C, $I_0 = 40$ pA

Hence option (B) is correct.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

SOL 3.44

Silicon is abundant on the surface of earth in the from of SiO_2.
Hence option (A) is correct.

SOL 3.45

$$\sigma_n = nq\mu_n$$
$$\sigma_p = pq\mu_p \qquad (n = p)$$
$$\frac{\sigma_p}{\sigma_n} = \frac{\mu_p}{\mu_n} = \frac{1}{3}$$

Hence option (B) is correct.

SOL 3.46

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

or
$$\frac{C}{A} = \frac{\varepsilon_0 \varepsilon_r}{d} = \frac{8.85 \times 10^{-12} \times 11.7}{10 \times 10^{-6}} = 10.35\,\mu\text{F}$$

Hence option (B) is correct.

SOL 3.47

In accumulation mode for NMOS having $p-$substrate, when positive voltage is applied at the gate, this will induce negative charge near $p-$ type surface beneath the gate. When V_{GS} is made sufficiently large, an inversion of electrons is formed and this in effect forms and $n-$ channel.
Hence option (B) is correct.

SOL 3.48

From the graph it can be easily seen that $V_{th} = 1$ V
Now $V_{GS} = 3 - 1 = 2$ V
and $V_{DS} = 5 - 1 = 4$ V
Since $V_{DS} > V_{GS} \longrightarrow V_{DS} > V_{GS} - V_{th}$
Thus MOSFET is in saturation region.
Hence option (C) is correct.

SOL 3.49

Trivalent impurities are used for making p type semiconductor. Boron is trivalent.
Hence option (C) is correct.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

SOL 3.50

Here emitter base junction is forward biased and base collector junction is reversed biased. Thus transistor is operating in normal active region.
Hence option (A) is correct.

SOL 3.51

We have $\beta = \dfrac{\alpha}{1-\alpha}$

Thus $\alpha \uparrow \rightarrow \beta \uparrow$
$\alpha \downarrow \rightarrow \beta \downarrow$

If the base width increases, recombination of carrier in base region increases and α decreases & hence β decreases. If doping in base region increases, recombination of carrier in base increases and α decreases thereby decreasing β. Thus S_1 is true and S_2 is false.
Hence option (D) is correct.

SOL 3.52

Hence option (C) is correct.

SOL 3.53

Applying KVL we get

$$V_{CC} - I_C R_C - V_{CE} = 0$$

or $$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{3 - 0.2}{1k} = 2.8 \text{ mA}$$

Now $$I_B = \frac{I_C}{\beta} = \frac{2.8\text{m}}{50} = 56\,\mu\text{A}$$

Hence option (A) is correct.

SOL 3.54

We know that

$$W_p N_A = W_n N_D$$

or $$W_p = \frac{W_n \times N_D}{N_A} = \frac{3\,\mu \times 10^{16}}{9 \times 10^{16}} = 0.3\,\mu\text{m}$$

Hence option (B) is correct.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

SOL 3.55

Conductivity $\sigma = nqu_n$

or resistivity $\rho = \frac{1}{\sigma} = \frac{1}{nq\mu_n}$

Thus $n = \frac{1}{q\rho\mu_n} = \frac{1}{1.6\times10^{-19}\times0.5\times1250} = 10^{16}/\text{cm}^3$

For n type semiconductor $n = N_D$

Hence option (B) is correct.

SOL 3.56

We know that

$$C_j = \left[\frac{e\varepsilon_S N_A N_D}{2(V_{bi}+V_R)(N_A+N_D)}\right]^{\frac{1}{2}}$$

Thus $C_j \propto \sqrt{\frac{1}{(V_{bi}+V_R)}}$

Now $\frac{C_{j2}}{C_{j1}} = \sqrt{\frac{(V_{bi}+V_R)_1}{(V_{bi}+V_R)_2}} = \sqrt{\frac{1}{4}} = \frac{1}{2}$

or $C_{j2} = \frac{C_{j1}}{2} = \frac{1}{2} = 0.5$ pF

Hence option (D) is correct.

SOL 3.57

Increase in gate oxide thickness makes difficult to induce charges in channel. Thus V_T increases if we increases gate oxide thickness. Hence S_1 is false.

Increase in substrate doping concentration require more gate voltage because initially induce charges will get combine in substrate. Thus V_T increases if we increase substrate doping concentration. Hence S_2 is false.

Hence option (C) is correct.

SOL 3.58

We know that

$$I_D = K(V_{GS} - V_T)^2$$

Thus $\frac{I_{DS}}{I_{DI}} = \frac{(V_{GS2} - V_T)^2}{(V_{GS1} - V_T)^2}$

Substituting the values we have

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

$$\frac{I_{D2}}{I_{D1}} = \frac{(3-1)^2}{(2-1)^2} = 4$$

or $$I_{D2} = 4I_{DI} = 4 \text{ mA}$$

Hence option (D) is correct.

SOL 3.59

$$E_g \propto \frac{1}{\lambda}$$

Thus $$\frac{E_{g2}}{E_{g1}} = \frac{\lambda_1}{\lambda_2} = \frac{1.1}{0.87}$$

or $$E_{g2} = \frac{1.1}{0.87} \times 1.12 = 1.416 \text{ eV}$$

Hence option (A) is correct.

SOL 3.60

Concentration gradient

$$\frac{dn}{dx} = \frac{10^{14}}{0.5 \times 10^{-4}} = 2 \times 10^{18}$$

$$q = 1.6 \times 10^{-19} C$$

$$D_n = 25$$

$$\frac{dn}{dx} = \frac{10^{14}}{0.5 \times 10^{-4}}$$

$$J_C = qD_n \frac{dn}{dx}$$

$$= 1.6 \times 10^{-19} \times 25 \times 2 \times 10^{18} = 8 \text{ A/cm}^2$$

Hence option (B) is correct.

SOL 3.61

Pentavalent make $n-$type semiconductor and phosphorous is pentavalent.

Hence option (D) is correct.

SOL 3.62

For silicon at 0 K $E_{g0} = 1.21$ eV

At any temperature

$$E_{gT} = E_{g0} - 3.6 \times 10^{-4} T$$

At $T = 300$ K,

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

$$E_{g300} = 1.21 - 3.6\times10^{-4}\times300 = 1.1 \text{ eV}$$

This is standard value, that must be remembered.
Hence option (B) is correct.

SOL 3.63

By Mass action law

$$np = n_i^2$$

$$p = \frac{n_i^2}{n} = \frac{1.5\times10^{16}\times1.5\times10^{16}}{5\times10^{20}} = 4.5\times10^{11}$$

Hence option (A) is correct.

SOL 3.64

Tunnel diode shows the negative characteristics in forward bias. It is used in forward bias.
Avalanche photo diode is used in reverse bias.
Hence option (C) is correct.

SOL 3.65

Hence option (D) is correct.

SOL 3.66

We that $R = \frac{\rho l}{A},\ \rho = \frac{1}{\sigma}$ and $\alpha = nqu_n$

From above relation we have

$$R = \frac{1}{nq\mu_n A}$$

$$= \frac{0.1\times10^{-2}}{5\times10^{20}\times1.6\times10^{-19}\times0.13\times100\times10^{-12}} = 10^6\Omega$$

Hence option (A) is correct.

SOL 3.67

$$\frac{dn}{dx} = \frac{6\times10^{16} - 10^{17}}{2\times10^{-4} - 0}$$

$$= -2\times10^{20}$$

Now $J_n = nq\mu_e E + D_n q\frac{dn}{dx}$

Since no electric field is present, $E = 0$ and we get

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

So, $J_n = qD_n \frac{dn}{dx}$

$= 1.6 \times 10^{-19} \times 35 \times (-2 \times 10^{20}) = -1120 \text{ A/cm}^2$

Hence option (D) is correct.

SOL 3.68

LED works on the principal of spontaneous emission.
In the avalanche photo diode due to the avalanche effect there is large current gain.
Tunnel diode has very large doping.
LASER diode are used for coherent radiation.
Hence option (C) is correct.

SOL 3.69

We know that $I = I_{o_{si}}\left(e^{\eta \frac{V_{D1}}{V_T}} - 1\right)$

where $\eta = 1$ for germanium and $\eta = 2$ silicon. As per question

$$I_{o_n}\left(e^{\frac{V_{Dsi}}{e^{\eta V_T}}} - 1\right) = I_{o_{Ge}}\left(e^{\eta \frac{V_{DGe}}{V_T}} - 1\right)$$

or $$\frac{I_{o_{si}}}{I_{o_{si}}} = \frac{e^{\eta \frac{V_{Dsi}}{V_T}} - 1}{e^{\eta \frac{V_{DGe}}{V_T}} - 1} = \frac{e^{2 \times \frac{0.718}{26 \times 10^{-3}}} - 1}{e^{2 \times \frac{0.1435}{26 \times 10^{-3}}} - 1} = 4 \times 10^3$$

Hence option (C) is correct.

SOL 3.70

$$E_g = \frac{hc}{\lambda} = \frac{6.626 \times 10^{-34} \times 3 \times 10^8}{54900 \times 10^{-10}} = 3.62 \text{ J}$$

In eV $$E_g(eV) = \frac{E_g(J)}{e} = \frac{3.62 \times 10^{-19}}{1.6 \times 10^{-19}} = 2.26 \text{ eV}$$

Alternatively

$$E_g = \frac{1.24}{\lambda(\mu\text{m})} \text{ eV} = \frac{1.24}{5490 \times 10^{-4} \mu\text{m}} = 2.26 \text{ eV}$$

Hence option (A) is correct.

SOL 3.71

We know that

$$I_D = K(V_{GS} - V_T)^2$$

Thus $$\frac{I_{D2}}{I_{D1}} = \frac{(V_{GS2} - V_T)^2}{(V_{GS1} - V_T)^2}$$

Substituting the values we have

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY ISBN: 9788192276236
Visit us at: www.nodia.co.in

$$\frac{I_{D2}}{I_{D1}} = \frac{(1.4-0.4)^2}{(0.9-0.4)^2} = 4$$

or $I_{D2} = 4I_{DI} = 4 \text{ mA}$

Hence option (D) is correct.

SOL 3.72

In $n-$well CMOS fabrication following are the steps :

(A) $n-$ well implant

(B) Source drain diffusion

(C) Metalization

(D) Passivation

Hence option (B) is correct.

SOL 3.73

For a JFET in active region we have

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

From above equation it is clear that the action of a JFET is voltage controlled current source.

Hence option (D) is correct.

SOL 3.74

At constant current the rate of change of voltage with respect to temperature is

$$\frac{dV}{dT} = -2.5 \text{ mV per degree centigrade}$$

Here $\Delta T = T_2 - T_1$

$= 40 - 20 = 20^\circ C$

Thus $\Delta V_D = -2.5 \times 20 = 50 \text{ mV}$

Therefore, $V_D = 700 - 50 = 650 \text{ mV}$

Hence option (B) is correct.

SOL 3.75

Condition for saturation is $I_C < \beta I_B$

Hence option (D) is correct.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

SOL 3.76

The metal area of the gate in conjunction with the insulating dielectric oxide layer and semiconductor channel, form a parallel plate capacitor. It is voltage controlled capacitor because in active region the current voltage relationship is given by

$$I_{DS} = K(V_{GS} - V_T)^2$$

Hence option (B) is correct.

SOL 3.77

In MOSFET the body (substrate) is connected to power supply in such a way to maintain the body (substrate) to channel junction in cutoff condition. The resulting reverse bias voltage between source and body will have an effect on device function. The reverse bias will widen the depletion region resulting the reduction in channel length. Hence option (D) is correct.

SOL 3.78

At a given value of v_{BE}, increasing the reverse-bias voltage on the collector-base junction and thus increases the width of the depletion region of this junction. This in turn results in a decrease in the effective base width W. Since I_S is inversely proportional to W, I_S increases and that i_C increases proportionally. This is early effect.
Hence option (C) is correct.

SOL 3.79

For an n-channel JEFT trans-conductance is

$$g_m = \frac{-2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= \frac{-2 \times 2 \times 10^{-3}}{-4}\left[1 - \frac{(-2)}{(-4)}\right]$$

$$= 10^{-3} \times \frac{1}{2} = 0.5 \text{ mho}$$

Hence option (B) is correct.

SOL 3.80

We have $$g_m = \frac{I_C}{V_T} = \frac{1}{26}$$

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

Now $$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

or $$400 = \frac{1/26}{2\pi(0.3 \times 10^{-12} + C_\mu)}$$

or $$(0.3 \times 10^{-12} + C_\mu) = \frac{1}{2\pi \times 26 \times 400} = 15.3 \times 10^{-12}$$

or $$C_\mu \; 15.3 \times 10^{-12} - 0.3 \times 10^{-12} = 15 \times 10^{-12} \; 15 \text{ pF}$$

Hence option (A) is correct.

SOL 3.81

For any semiconductor (Intrinsic or extrinsic) the product $n\,p$ remains constant at a given temperature so here

$$np = n_i p_i$$

Hence option (D) is correct.

SOL 3.82

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

Hence option (D) is correct.

SOL 3.83

For a Forward Bias p-n junction, current equation

$$I = I_0(e^{V/kT} - 1)$$

or $$\frac{I}{I_0} + 1 = e^{V/kT}$$

or $$kT\log\left(\frac{I}{I_0} + 1\right) = V$$

So if we plot $\log I$ vs V we get a straight line.
Hence option (B) is correct.

SOL 3.84

A specimen of $p-$ type or $n-$ type is always electrical neutral.
Hence option (B) is correct.

SOL 3.85

Hence option (C) is correct.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

SOL 3.86

The unit of q is e and unit of kT is eV. Thus unit of e/kT is $e/eV = \text{V}^{-1}$.
Hence option (B) is correct.

SOL 3.87

Hence option (D) is correct.

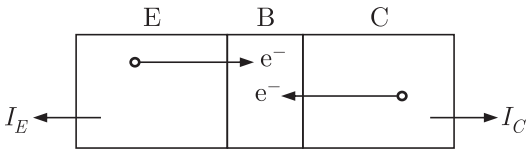
SOL 3.88

We have $n_i = 1.5 \times 10^{10}/\text{cm}^3$
$N_d = 2.25 \times 10^{15}\,\text{atoms/cm}^3$
For n type doping we have electron concentration
$$n \simeq N_d = 2.25 \times 10^{15}\,\text{atom/cm}^3$$
For a given temperature
$$np = n_i^2$$
Hole concentration
$$p = \frac{n_i^2}{n}$$
$$= \frac{(1.5 \times 10^{10})^2}{2.25 \times 10^{15}} = 1.0 \times 10^5/\text{cm}^3$$
Hence option (C) is correct.

SOL 3.89

In pn-junction isolated circuit we should have high impedance, so that pn junction should be kept in reverse bias. (So connect p to negative potential in the circuit)
Hence option (D) is correct.

SOL 3.90



If both junction are forward biased and collector base junction is more forward biased then I_C will be flowing out wards (opposite direction to normal mode) the collector and it will be in reverse saturation mode.
Hence option (B) is correct.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

SOL 3.91

For normal active mode we have

$$\beta = \frac{I_C}{I_B}$$

For small values of I_C, if we increases I_C, β also increases until we reach (I_C) saturation. Further increases in I_C (since transistor is in saturation mode know) will increases I_B and β decreases.
Hence option (C) is correct.

SOL 3.92

For a n-channel mosfet thresholds voltage is given by

$$V_{TN} = V_{GS} - V_{DS}(\text{sat})$$

for p-channel [p^+ polysilicon used in gate]

$$V_{TP} = V_{SD}(\text{sat}) - V_{GS}$$

so $$V_{TP} = - V_{DS}(sat) + V_{GS}$$

so threshold voltage will be same.
Hence option (C) is correct.

SOL 3.93

Emitter current is given by

$$I_E = I_0(e^{V_{BE}/kT} - 1)$$

or $$I_E = I_0 e^{V_{BE}/kT} \qquad e^{V_{BE}/kT} >> 1$$

or $$V_{BE} = kT\ln\left(\frac{I_E}{I_0}\right)$$

Now $$(V_{BE})_1 = kT\ln\left(\frac{I_{E1}}{I_0}\right)$$

$$(V_{BE})_2 = kT\ln\left(\frac{I_{E2}}{I_0}\right)$$

or $$(V_{BE})_2 - (V_{BE})_1 = kT\left[\ln\left(\frac{I_{E2}}{I_{E1}}\right)\right] = kT\ln\left(\frac{2I_{E1}}{I_{E1}}\right)$$

Now if emitter current is double i.e. $I_{E2} = 2I_{E1}$

$$(V_{BE})_2 = (V_{BE})_1 + (25 \times 0.60)\,\text{m volt}$$
$$= (V_{BE})_1 + 15\,\text{m volt}$$

Thus if emitter current is doubled the base emitter junction voltage is increased by 15 mV.
Hence option (C) is correct.

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

SOL 3.94

Unity gain frequency is given by

$$f_T = f_B \times \beta = 10^6 \times 200 = 200\,\text{MHz}$$

α-cutoff frequency is given by

$$f_\alpha = \frac{f_\beta}{1-\alpha} = \frac{f_\beta}{1-\dfrac{\beta}{\beta+1}} = f_\beta(\beta+1)$$

$$= 10^6 \times (200+1) = 201\,\text{MHz}$$

Hence option (A) is correct.

SOL 3.95

Hence option (A) is correct.

****

GATE Previous Year Solved Paper By RK Kanodia & Ashish Murolia
Published by: NODIA and COMPANY **ISBN:** 9788192276236
Visit us at: www.nodia.co.in

Exclusive Series By Jhunjhunuwala

GATE CLOUD

By R. K . Kanodia & Ashish Murolia

GATE Cloud is an exclusive series of books which offers a completely solved question bank to GATE aspirants. The book of this series are featured as

- Over 1300 Multiple Choice Questions with full & detailed explanations.
- Questions are graded in the order of complexity from basic to advanced level.
- Contains all previous year GATE and IES exam questions from various branches
- Each question is designed to GATE exam level.
- Step by step methodology to solve problems

Available Title In this series

- Signals and Systems (For EC and EE)
- Network Analysis (For EC)-- Available in 2 Volumes
- Electric Circuit and Fields (For EE) -- Available in two volumes
- Electromagnetic (For EC)

Upcoming titles in this series

- Digital Electronics (Nov 2012)
- Control Systems (Dec 2012)
- Communication Systems (Jan 2012)

For Sample chapter please mail to enquiry@nodia.co.in or visit www.nodia.co.in

Exclusive Series By Jhunjhunuwala

GATE GUIDE

Theory, Example and Practice

By R. K . Kanodia & Ashish Murolia

GATE GUIDE is an exclusive series of books which provides theory, solved examples & practice exercises for preparing for GATE. A book of this series includes :

- **Brief and explicit theory**
- **Problem solving methodology**
- **Detailed explanations of examples**
- **Practice Exercises**

Available Title In this series

- Signals and Systems (For EC and EE)
- Network Analysis (For EC)
- Electric Circuit and Fields (For EE)

Upcoming titles in this series

- Digital Electronics(For EC and EE)
- Control Systems (For EC and EE)
- Communication Systems (For EC and EE)

For Sample chapter please mail to enquiry@nodia.co.in or visit www.nodia.co.in