ANNA UNIVERSITY – 2007

B.E/B.TECH DEGREE EXAMINATION

DIGITAL SYSTEM

(ELECTRICAL & ELECTRONICS ENGINEERING)

TIME-3HOUR
MARK-100

ANSWER ALL QUESTIONS

PART A (10 X 2 = 20)

1. Why binary number system is used in digital system.

2. Represent the following numbers in 2's complement from

(i) +3 (ii) +25 (iii) –5 (iv) -11

3. Obtain the following operations using only NAND gates

(a) NOT (b) AND

4. Define the laws of Boolean Algebra.

5. Why TTL is preferred over DTL?

6. What are half and full adders?

7. Define the term triggering the flip flops

8. Distinguish the classification of sequential circuits.

9. Define Mask Programmable PLA and Field Programmable PLA.

10. Give the logic table of a ROM which will multiply two 2-bit binary numbers.

PART B (5 X 16 = 80)

11.i) Specify the radix and the symbols used in (1) binary (2) ternary (3) quinary (4) octal and (5) hexadecimal number system.

ii) Convert (329.678)10 to an equivalent number in base 6 having a conversion error less than .001.

iii) Design a parity generator to generate an odd parity bit for a 4-bit word. Use EX-OR and EX-NOR gates.

12.a) Use Quine-Mccluskey method to obtain the minimal sum for the following function.
F(X1 X2 X3 X4) = ? (0, 1, 3, 6, 7, 14, 15)

OR

12.b)i) Simplify the function using Karanaugh map.

1) F(A, B, C, D) = ?(0, 1, 2, 4, 5, 7, 11, 15)

2) F(W, X, Y,Z) = ?(2, 3, 10, 11, 12, 13, 14, 15)

ii) Implement the following function with either NAND or NOR gates. Use only 4 gates. Only the normal inputs are available. (1) d= wyz (2) F = w' xz+w' yz+x'+wx y'z.

13.a)i) Construct a DTL NAND gate and explain.

ii) Design a combinational circuit that compares two 4-bit numbers A and B to check if they are equal or not.

OR

13.b) Create the truth table for logic that receives BCD digit as input and provides 7 outputs to drive a 7 segment display. Using the don't cares, obtain the reduced Boolean expression for the 'b" and 'e' segments output of a 7 segment display driver.

14.a) A sequential circuit has two JK flip flops A and B, the inputs, X and Y and one output, Z. The flip flop input function and the circuit output functions are as follows.
JA = Bx + B'y' KA = B'xy'
JB = A'x' KB = A + xy'

1) Draw logic diagram (2) Tabulate the state table (3) Derive the next state equation for A and B.

OR

14.b) List the PLA program table for the BCD to excess 3 code converter circuit and show its implementation for any two output functions.

15.a) Analyze the circuit shown in Fig.1. Obtain the state table and the state diagram and determine the function of the circuit.

OR

15.b)i) Implement the function F(X1, X2, X3, X4) = ? (0, 1, 3, 4, 8, 9, 15) with an 8 x 1 multiplexer where the following variables are connected in the specified order to selection lines S2 S1 and S0 respectively.

1) X1, X2, X3 (2) X2, X3, X4

ii) Describe the working of a BCD ripple counter with neat circuit diagram.