ANNA UNIVERSITY – 2006

B.E/B.TECH III SEMESTER DEGREE EXAMINATION

DIGITAL SYSTEM DESIGN

(INFORMATION TECHNOLOGY)

TIME-3HOUR
MARK-100

ANSWER ALL QUESTIONS

PART A (10 * 2 = 20)

1. List the first 16 numbers in base 12. Use the letters A and B to represent the last two digits. Convert the numbers (546)12 to base 8.

2. Using DeMorgan's theorem, convert the following Boolean expression to an equivalent expression that has only OR and complement operations. Show that the function can be implemented with logic circuits that have only OR gates and inverters:
F = (y+z') (x+y) (y'+z)

3. A combinational switching network has 4 inputs (A, B, C, D) and one output F. F
= 0 if 3 or 4 of the inputs are 0.
· Write the maxterm expansion for F.
· Using AND and OR gates, find a minimum three-level network to realize F.

4. What do you mean by positive logic, negative logic and mixed logic?

5. Realize the operation of a full adder using a 3x8 decorder.

6. Implement the following function with a multiplexer:
F(A, B, C, D) = ?(0, 1, 3, 4, 8, 9, 15)
Use B,C and D as select lines.

7. With the help of a block diagram, explain the operation of a J-K Master-Slave Flip flop.

8. Draw the logic diagram of a D Flip-flop using NAND gates and derive its characteristic table.

9. What are the guidelines to be followed while making state assignments?

10. What are hardware description languages?

PART B (5 * 16 = 80)

11. i) In what way is the Quine-McCluskey method advantages over the Karnaugh method of simplifying a Boolean function?

ii) Simplify the given Boolean function using Quine-McClukey, method: ? (w,x,y,z) = ? (1,4,6,7,8,9,10,11,15)

12a. i) Which are functionally complete sets of logic gates? Explain.

ii) How are AND, OR and NOT operations realized with NAND gates?

iii) Using AND and OR gates, find a minimum network to realize f(a,b,c,d) = M1M2M5M9M10M14 using two-level logic and three-level logic.

(OR)

12b. i) Convert the following network to all NAND gates, by adding bubbles and inverters where necessary.

ii) Convert to all NOR gates.

13a. i) Discuss the usage of multiplexers in digital systems.

ii) Explain with the help of a block diagram, a quadruple 2-to-1 line multiplexer.

(OR)

13b. Realize the functions given below using a PLA. Give the PLA table and internal connection diagram for the PLA:

F1 (a,b,c,d) = ? (1,2,4,5,6,8,10,12,14)
F2 (a,b,c,d) = ? (2,4,6,8,10,11,12,14,15)

14a. Design a counter which counts the following sequence:
0,8,12,10,14,19,13,11,15,0,8,12, …. Use clocked J-K flip flops and NAND gates.

(OR)

14b. i) Specify the method that is used to construct a state table.

ii) Describe with suitable examples, the two types of clocked-sequential networks.

15a. i) What is an SM chart? In what way is it different from an ordinary flow chart?

ii) Derive the SM chart for a binary multiplier control and explain the sequences indicated in the chart.

(OR)

15b. i) Describe with suitable examples, the different conditions that can occur in a network.

ii) With suitable examples, explain the hazards in combinational networks.