2006-PUNJAB TECHNICAL UNIVERSITY
B.TECH III SEMESTER DEGREE EXAMINATION
DIGITAL CIRCUIT AND LOGIC DESIGN
(COMPUTER SCIENCE ENGINEERING)

TIME-3HOUR

MARKS-60

NOTE: SECTION A IS COMPULSORY. ATTEMPT ANY FOUR QUESTIONS FROM SECTION B AND TWO FROM SECTION C

SECTION A MARKS 2 EACH

1 (a) What four bit number is equal to its 2's complement ?

(b) Discuss the significance of Boolean Logic.

(c) What are the low and high levels at the input and output sides of a TTL logic?

(d) Explain the term tri-state.

(e) Discuss the racing condition. How is it avoided?

(f) What are the functions of the counter?

(g) Justify the need of bus technology.

(h) Comare the level triggering and edge triggering.

(i) What is the difference between accuracy and resolution for A-D convertors?

(j) List the merits and applications of CAD tools.

SECTION B MARKS 5 EACH

2. Minimise the following logic function and realize using NAND gates:
$f(A,B,C,D)=SIGMA\ m(1,3,5,8,9,11,15) + d(2,13)$

3. Compare the features of various logic families.

4. Describe the salient features os VLSI design.

5. Explain with an example the parallel comparator type A-D convertor.

6. Compare the features of ROM, RAM, EEPROM, PLA and PAL..

SECTION C MARKS 10 EACH

7. Design a mod Counter. Completely show the timing waveforms indcating counting and division of frequency.

8. Write short notes on any three of the following:

(a) Transmission line effects.
(b) programmable logic devices.
(c) Astable multivibrator
(d) Computer aids in synthesis.

9. A sequential circuit is to have two levels inputs x1 and x2 and one clock. An output pulse Z is to be coincident with a clock pulse occuring with $=x1x2 =01$ immideately following two or more consecutives clock pulses with $x1x2=10$ and $x1x2 =00$. $x1x2=11$ can never occur. draw the stable state diagram and design the circuit using minimum number of J-K flip-flops.