2008-COCHIN UNIVERSITY OF SCIENCE AND TECHNOLOGY

II B.TECH MODEL EXAMINATION

LOGIC DESIGN

(ELECTRONICS AND COMMUNICATION ENGINEERING)

TIME-3HOUR
MARKS-60

MAY-2008

ANSWER ALL QUESTIONS

SECTION A [5*4=20]

1. Show the multiplication of binary 10101 by 11010

2. Explain what is mean by PAL and PLA

3. Briefly explain the different logic families

4. Implement a half adder using NAND only

5. Explain briefly astable multivibrator.

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SECTION B [2*20=40]

6. a) Simplify the following equation using K-map V=f(a,b,c,d)= m(2,3,4,5,13,15) + d (8,9,10,11)

b) Draw the logic symbol and truth table of a half subtractor

OR

7. a) Draw a neat diagram and explain a carry look ahead adder.

b) Explain the block diagram of a parallel binary multiplier.

8. a) Explain two input TTL NAND gate.

b) Compare totem pole and open collector.

OR

9. a) Explain interfacing of TTL to CMOS & CMOS to TTL .

b) Explain ECL NOR/OR gate.

c) Explain following terms

1. Noise margin

2. FAN OUT

3. FAN IN

4. Propagation delay.