# 2005-ANDHRA UNIVERSITY

## II B.TECH I SEMESTER DEGREE EXAMINATION

## DIGITAL LOGIC DESIGN

## (INFORMATION TECHNOLOGY)

TIME-3HOUR
MARKS-70

**NOTE:SECTION A IS COMPULSORY.ATTEMPT ANY FOUR QUESTIONS FROM SECTION B.**

**SECTION A [5*2=10 MARKS]**

1. a) Given that (79)10 = (142)b determine the value of b.

b) Rewrite the following expression in a form that requires as few inversions as possible b'c + acd' +a'c +c(a+c)(a'+d')

c) Represent the function (x,y,z)=y using Kamangh Map.

d) Explain the behavior of the following logic circuit with input A and output B

e) Realize an Inverter and Buffer using Half-Adder

**SECTION B [4*15=60 MARKS]**

2. a) In a certain number system, X and Y are two successive digits. When written as XY, it is equal to 25 and when written as YX, it is equal to 31 in decimal system. Find the base of the system Also find the values of X and Y.

b) Construct one of the error detecting codes for single digit BCD numbers and Hexadecimal numbers.

3. Demonstrate, without using perfect induction, whether or not each of the following is valid. a) (x+y) (x+y') (x'+y)(x'+y')=0 b) a'b+b'c+c'a=ab'+bc'+ca' c) ab+a'c+bcd = ab + a'c

b) Write the HDL description of the circuit specified by the following Boolean functions:

x = A(CD+B) + BC'
y = (AB' + A'B)C + D')
z = [(A+B)(C'+D'B)]'

4. Given the function T (w,x,y,z) = S (1,3,4,5,7,8,9,11,14,15)

a) Use the K - map to determine the set of all prime implicants. Indicate specifically the essential ones. Find three distinct minimal expressions for T.

b) Assume that only unprimed variables are available. Construct a circuit which realizes T.

5. a) Design a combinational circuit that multiplies two 2-bit numbers. a1ao and b1bo, to produce a 4-bit product c3c2c1c0. Use AND gates and half-adder.

b) Design a combinational circuit that has four inputs and four outputs. The output generates the 2;s complement of input binary number.

6. Design a sequential circuit specified by the state diagram given below using T Flip-Flops. DIAGRAM

b) Draw and explain the logic diagram of a master-slave D flip-flop using NAND gates.

7. a) Design a synchronous BCD counter with JK flip-flops.

b) Design a shift register with parallel load that operates according to the following function table:

Shift Load Register Operation
0 0 No Change
0 1 Load Parallel Data
1 X Shift Right

8. Write short notes on the following

a) Programmable Array Logic

b) Asynchronous Sequential Logic

c) HDL for registers and Counters

d) D-latch and D-Flip-Flop