XII HSC - BOARD - MARCH - 2017

Date: 22.03.2017

COMPUTER SCIENCE - II (D-9)

SOLUTIONS

1. (A)

(a) (iv) 5

Topic:Introduction to Microprocessors and Organization of 8085 ; Sub-topic:Flags_Target-2017_XII–HSC Board Exam __Computer Science-II

(b) (ii) Logical

Topic: Instruction Set and Programming of 8085; Sub-topic:Instruction_Target-2017_XII–HSC Board Exam __Computer Science-II

(c) (iii) 16 MB

Topic:Introduction to Intel X-86 Family; Sub-topic:Microprocessor__Target-2017_XII–HSC Board Exam __Computer Science-II

(d) (i) Fiber Optic

Topic:Networking Technology; Sub-topic:Cable_Target-2017_XII–HSC Board Exam __Computer Science-II

(B)

(a) **(i) Multiplex Address/Data Bus AD_0-AD_7**

(1) The signal lines AD0 to AD7 are bidirectional. They Serve a dual purpose. They are used as the low-order address buse as well as the data bus.

(2) In executing an instruction, during the earlier part of the cycle, these lines are used as the low - order address bus. During later part of the cycle, these lines are used as the data bus.

(3) However, the low-order address bus can be separated from these signals by using a latch.

(ii) RST 6.5 :

(1) **RESTART INTERRUPT :** This signal is used to interrupt the microprocessor.

(2) When an interrupt is recognized the next instruction is executed from a fixed location is the memory i.e. $6.5 \times 8 = 0034\,H$.

(3) It is **maskable** interrupt.

(4) They cause an internal restart to be automatically insert.

(iii) CLK (OUT) :

(1) The whole circuitry is synchronized with clock

(2) The speed of the system depends on the clock frequency.

Topic: Instruction Set and Programming of 8085; Sub-topic:Instruction_Target-2017_XII–HSC Board Exam __Computer Science-II

(b) (i) Immediate Addressing Mode
2 bytes
(ii) Register Indirect Addressing Mode
1 byte
(iii) Direct Addressing Mode
3 bytes

Topic:Introduction to Microprocessors and Organization of 8085 ; Sub-topic:Addressing Mode_Target-2017_XII–HSC Board Exam __Computer Science-II

(c) **Twisted Pair Cable:**

(1) It consists of a pair of wires or one or more pairs of two twisted copper wires.
(2) This is inexpensive medium.
(3) EMI effect is maximum.
(4) Attenuation is more than coaxial cable.
(5) Bandwidth capacity is from 1 to 100 Mbps upto 100 mtrs.
(6) They can be used only for short distance communication.

Coaxial Cable:

(1) It is a shallow cable with a solid copper at the center of the cable surrounded by plastic form insulation.
(2) Relatively expensive i.e. twice or thrice than twisted pair.
(3) EMI effect is minimum.
(4) Attenuation is less than twisted pair cable.
(5) Bandwidth capacity is from 500 Mbps upto 100 mtrs.
(6) It is commonly used in network.

Topic:Networking Technology; Sub-topic:Cable_Target-2017_XII–HSC Board Exam __Computer Science-II

2. (A)

(a) **(i) T-State**

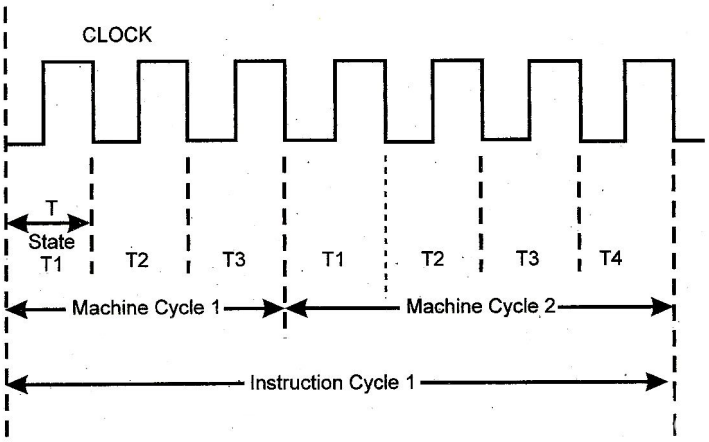
The subdivision of an operation, which is performed in one clock period is called as T-state.

(ii) Machine cycle

Machine cycle is defined as the time required to complete any operation of accessing either memory or I/O which is the subpart of an instruction. In 8085, the machine cycle may consist of three to six T-states.

(iii) Instruction cycle

An instruction cycle is defined as the time required to complete the execution of an instruction. The 8085 instruction cycle consists of one to five machine cycle.



The above diagram shows machine cycles, T-states and instruction cycle required for execution of an instruction. From it is clear that an instruction cycle consists of number of machine cycles and a machine cycle consists of number of T- states.

Topic: Instruction Set and Programming of 8085; Sub-topic:Instruction Cycle_Target-2017_XII–HSC Board Exam __Computer Science-II

(b) **Wireless Media:** Transmission of waves take place in the electromagnetic (EM) spectrum. The carrier frequency of the data is expressed in cycles per second called hertz (Hz). Low freqeuncy signals can travel for long distances through many obstacles but can not carry a high bandwidth of date while high frequency signals can travel for shorter distances through few obstacles and carry a narrow bandwidth. Also the noise effect on the signal is inversely proportional to the power of the radio transmitter.

Advantages of Wireless Media

(1) The advantage of wireless media is high data rates by using large bandwidth which can give transmission speed around 24 Kbps.

(2) By this media the communication can reach rural and hilly areas.

(3) Bandwidth for digital data 1 to 100 Mbps.

Topic:Networking Technology; Sub-topic:Wireless Media_Target-2017_XII–HSC Board Exam __Computer Science-II

(c) (i) ADD E: ADD E with Accumulator

Before execution : [A] = 71H

instruction : ADD E

71 H = 0 1 1 1 0 0 0 1

ADD 39 H = 0 0 1 1 1 0 0 1

1 0 1 0 1 0 1 0 = AA H

After execution [A] = AA H

[Cy] = 00H

(ii) ORA E : Logically OR with Acc

Before execution : [A] = 71H

Instruction : ORA E

71 H = 0 1 1 1 0 0 0 1

ORA 39 H = 0 0 1 1 1 0 0 1

0 1 1 1 1 0 0 1 = 79 H

After execution : [A] = 79H

(iii) RRC : Rotate accumulator right by one bit.

Before execution : [A] = 71H 0 1 1 1 0 0 0 1

Instruction : RRC

After execution [A] = 1 0 1 1 1 0 0 0 = B8 H

$\therefore [A] = B8H$

[Cy] = 01H

Topic: Instruction Set and Programming of 8085; Sub-topic:Instruction_Target-2017_XII–HSC Board Exam __Computer Science-II

(B)

(a)

(1) A microcontroller is a complete microprocessor system, consisting of microprocessor, limited amount of ROM or EPROM, RAM and I/O ports, built on a single integrated circuit.

(2) Microcontroller is infact a microcomputer, but it is called so because it is used to perform control functions.

(3) The designer of a microcontroller identify all the needs to build simple microprocessor system and puts as many as possible in single IC.

e.g. Intel's 8048, 8051

Advanced Features of 8052 Microcontroller over 8051 Microcontroller

(1) Microcontroller 8051 has 4k bytes of ROM, whereas 8052 has 8k bytes of onboard ROM or EPROM.

(2) Microcontroller 8051 has 128 bytes of RAM, whereas 8052 has 256 bytes of onboard RAM.

(3) Microcontroller 8051 has a dual 16-bit timer event counter whereas 8052 has an extra 16-bit timer event counter.

(4) The cost of microcontroller 8051 is less than that of microcontroller 8052.

(5) Both 8051 and 8052 are used in high volume applications and both allow us to write large program. But in 8052 we can write larger programs than that in 8051.

Topic:Introduction to Microcontroller; Sub-topic:Features_Target-2017_XII–HSC Board Exam __Computer Science-II

(b)

* An interrupt is a subroutine called, initiated by external device through hardware (hardware interrupt)

* An interrupt can also be viewed as a signal, which suspends the normal sequence of microprocessor and then microprocessor gives service to that device which has given the signal. After completing the service, microprocessor again returns to the main program.

(1) 8085 provides 5 hardware interrupts:

(i) TRAP (ii) RST 7.5 (ii) RST 6.5 (iv) RST 5.5 (v) INTR

(2) These interrupts are vectored interrupts. It means that when these interrupts are given , it is directed (or vectored) to transfer the control to specific memory location given by

TRAP $= 4.5 \times 8 = 0024\,H$ RST $7.5 = 7.5 \times 8 = 003\,C$ H

RST $6.5 = 6.5 \times 8 = 0034$ H RST $5.5 = 5.5 \times 8 = 002\,C$ H

(3) Among these interrupts, TRAP is non- maskable interrupt which can not be disabled. But the other four interrupts are maskable interrupts, which can be disabled.

(4) The TRAP has highest priority and the INTR has lowest priority among the hardware interrupts. The hardware interrupts in descending order of priority are listed below:

(i) TRAP - **highest priority** (ii) RST 7.5 (iii) RST 6.5 (iv) RST 5.5

(v) INTR - **lowest priority.**

Topic:Introduction to Microprocessors and Organization of 8085 ; Sub-topic:Interrupts_ Target-2017_XII–HSC Board Exam __Computer Science-II

3. (A)

(a)

	Memory mapped I/O	I/O mapped I/O
1.	I/O is assigned to the separate address space of memory.	I/O is assigned with same address of memory.
2.	Separate control signal is not required.	It is required like IO/M.
3.	Memory space is reduced due to insertion of I/O address.	Full memory space can be used.
4.	It requires 16-bit address bus.	It uses 8-bit address bus only.

Topic:Introduction to Microprocessors and Organization of 8085 ; Sub-topic:Addressing I/O Devices_Target-2017_XII–HSC Board Exam __Computer Science-II

(b) (i) PUSH PSW : [PUSH ACCUMULATOR AND FLAG REGISTER ON STACK]

Format: [[SP] - 1] ← [A]

$[[SP]-2]_0 \leftarrow [Cy],\quad [[SP]-2]_1 \leftarrow x,$

$[[SP]-2]_2 \leftarrow [P],\quad [[SP]-2]_3 \leftarrow x,$

$[[SP]-2]_4 \leftarrow [Ac],\quad [[SP]-2]_5 \leftarrow x,$

$[[SP]-2]_6 \leftarrow [Z],\quad [[SP]-2]_7 \leftarrow [S],$

$[SP] \leftarrow [SP]-2 \qquad (x - \text{Undefined})$

Addressing: Register indirect addressing

Bytes : 1 byte

Flag : None

Comment:

(1) The content of accumulator are moved to the memory location, whose address is one less than the content of stack pointer.

(2) The content of processor status word (flag register) are moved to the memory location, whose address is two less than the content of stack pointer.

(3) The stack pointer is decremented by 2

Example: Let [A] = 33 H and Flag Register = 25 H, [SP] = D015

Instruction: PUSH PSW

After execution : [D014] = 33 H, [D013] = 25H

[SP] = D013 H

(ii) **INX rp**: [INCREMENT REGISTER PAIR BY 1]

Format: $[rp] \leftarrow [rp] + 1$

Addressing: Register addressing

Group: Arithmetic group

Bytes: 1 byte

Flag: None

Comment: This instruction increments the content of register pair rp by 1. No flags are affected. The instruction views the contents of the two registers as a 16-bit number.

Example: Let [HL] = D000 H

Instruction : INX H

After execution : [HL] = D001 H

(iii) **DAD rp :** [ADD REGISTER PAIR TO H AND L REGISTER]

Format: $[H][L] \leftarrow [H][L] + [rh][rI]$

Addressing: Register addressing

Group: Arithmetic group

Bytes: 1 byte

Flag: Cy

Comment: The contents of register pair rp are added to the contents of H-L pair. Result is placed in register H and L. Only carry flag is affected.

Example: Let $[H] = 03\,H, [L] = 05, [D] = 15\,H$ and $[E] = 12\,H$

Instruction: DAD D

After execution: $[L] = 05 + 12 = 17\,H$

$[H] = 03 + 15 = 18\,H$

$\therefore [H - L] = 1817\,H$

In this case, carry flag is reset.

Topic: Instruction Set and Programming of 8085; Sub-topic:Instruction_ Target-2017_XII–HSC Board Exam __Computer Science-II

(c) (1) Computer store digital data, while telephone lines can only transfer analog data. If a computer is to be connected to internet through telephone, then it must convert digital data to analog data before transmitting the computer signals.

(2) Converting one signal form to another form is called modulation and reconverting it to original form is called as demodulation.

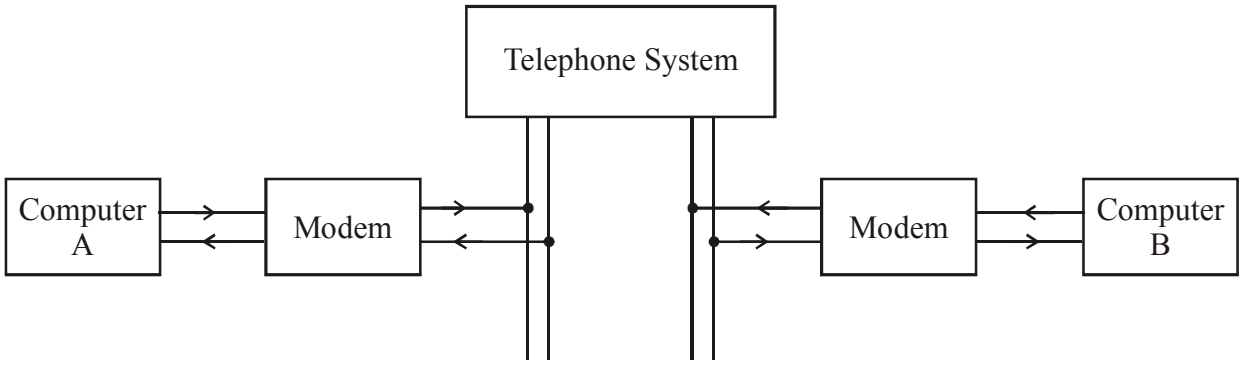
(3) Modern is modulator/demodulator. Modem is used to connect computer to internet. Modems convert digital data to analog data and vice-a-versa.

(4) They have two advantages:

(a) Modem allows higher speed of transmission on any given analog line.

(b) Modem reduce effect of noise and distortion.

(5) The function of modem is described by following figure.



(6) Modems are classified into two categories according to transmission method:
(a) Asynchronous modems
(b) Synchronous modems

Topic:Networking Technology; Sub-topic:Modem_Target-2017_XII–HSC Board Exam __Computer Science-II

(B)

(a) (i) **8048**

(1) Intel's first microcontroller was 8048. The 8048, 8049 and 8050 all have indentical architectures with the exception of memory size.

(2) In each case, the memory doubles. 8048 supports 1K byte of internal memory.

(3) 8048 has 64 bytes internal RAM, including 32 bytes of register/memory location.

(4) The microcontrollers are low cost products and hence are very popular.

(ii) **8052**

(1) 8052 is a simple expansion of 8051

(2) 8052 has 8K bytes of onboard ROM and 256 bytes of onboard RAM.

(3) 8052 allows programmers to write larger programs and that can use more data.

(4) The cost of 8052 is more than that of 8051.

(5) The 8052 also has one extra 16-bit counter-time. This counter-time gives more flexibility.

(iii) **8031**

(1) The alternative versions of 8051 and 8052 are 8031 and 8032.

(2) These devices do not have any on board ROM. It may use external ROM for program memory.

(3) These are excellent devices for prototyping and low-volume products.

(iv) **8050**

(1) Intel's first microcontroller was 8048. The 8048, 8049 and 8050 all have indentical architectures with the exception of memory size.

(2) In each case, the memory gets doubles. 8050 supports 4K bytes of internal memory.

(3) 8050 have a total of 128 and 256 bytes of RAM.

(4) The microcontrollers are low cost products and hence are very popular.

Topic:Introduction to Microcontroller; Sub-topic:Features_Target-2017_XII–HSC Board Exam __Computer Science-II

(b) (1) Ethernet is a local area network technology, with networks tradionally operation within single building.

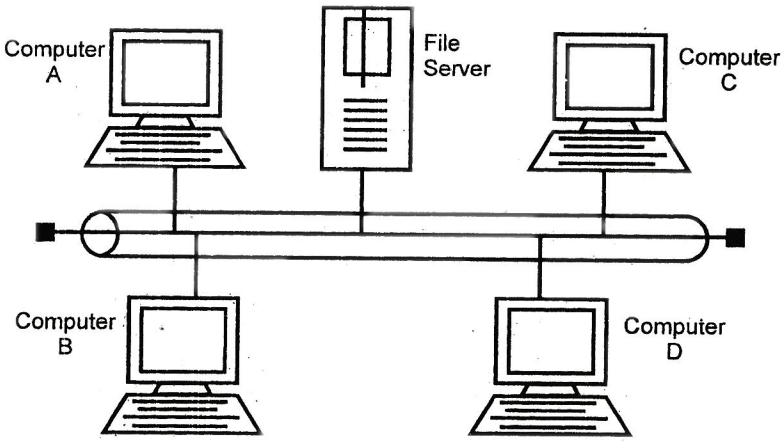
(2) Atmost, Ethernet devices can have a few hundred meters of cable between them. Modern technology allows Ethernet to span upto 10 kms.

(3) Ethernet devices are connected to a common shared medium that provides the path along which the electronic signals will travel. Historically, this medium was co-axial cable. But, now-a-days twisted pair cable or fibre optic cable are also used.

(4) Ethernet network transmit data in small units called **frames.**

(5) Each frame must contain source address as well as destination address, which identifies recipient and sender of message. The address will uniquely indentify node. No two Ethernet devices can have same address.

(6) Ethernet network is as shown in following in figure.



In above figure when computer A sends message to computer C, computer B and D will also get the message and check whether the destinations address mathches to its own address or not, if not, it will discard the frame.

Ethernet Types:

- 10 BASE 5 : Speed 10 Mbps (10) and thick co-axial known as thicknet. Maximum cable net 500 mtrs.(5).
- 10 BASE 2 : Speed 10 Mbps (10) and thin co-axial cable known as thinnet. Maximum length 200 mtrs. (2)
- 10 BASE T : Speed 10 Mbps (10) and uses UTP twisted pair 100 mtrs.
- 10 BASE FL : Speed 10 Mbps(10) uses (FL).
- 100 BASE VG : Speed 100 Mbps (10) twisted pair. (VG-Voice Grade)

Topic:Networking Technology; Sub-topic:Ethernet_Target-2017_XII–HSC Board Exam __Computer Science-II

4. (A)

(a) **80386 :**

(1) The INTEL's 80386 is a 32-bit microprocessor introduced in 1985.

(2) 80386 is a logical extension of 80286. It is more highly pipelined.

(3) The instruction set of 80386 is a superset of other members of 8086 family.

(4) It has 32-bit data bus and 32-bit nonmultiplexed address bus. It can address a physical memory of 2^{32} i.e. 4 Gbytes. The 80386 memory mangement allows it to address 2^{46} or 64 Tbytes.

(5) The 386 can be operated in one of the following memory management modes:

(a) Paged mode

(b) Non- paged mode.

(6) When operated in paged mode, the 386 switches the paging unit then after the segment unit. The paging unit allows memory pages of 4 KB each to be swapped in and out from disk. In non - paged mode, memory mangement unit operates very similar to the 286.

(7) Virtual addresses are represented with selected components and an offset component as they are with 80286.

80486 :

(1) Intel's 80486 is a 32-bit microprocessor. It has 32-bit address bus and 32-bit data bus. It was introduced in 1989.

(2) The 486 is basically a large integral circuit which contains a fast built-in, a math coprocessor, a memory mangement unit (M.M.U), and an 8 kbyte cache memory.

(3) 80486 has DX and SX versions.

(4) All 486 processor have 32-bit data bus. SX version does not have on chip- numeric coprocessor.

(5) The 486 achieves its high speed operation from its faster clock speeds, internal pipe lined architecture and the use of reduced instruction set computing (RISC) to speed up the internal microcode.

(6) 486 also has 486 DX2 and 486 DX4 versions, with double and triple clock speed.

Topic:Introduction to Intel X-86 Family; Sub-topic:Attributes__Target-2017_XII–HSC Board Exam __Computer Science-II

(b) Following are the instructions make accumulator content clear:

(1) ANI 00H
(2) XRA A
(3) SUB A
(4) MVI A, 00H

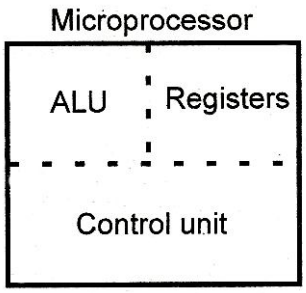
Topic: Instruction Set and Programming of 8085; Sub-topic:Instruction_Target-2017_XII–HSC Board Exam __Computer Science-II

(c) (i) Microprocessor is a semiconductor, multipurpose, programmable logic device that reads binary instructions from a storage device called memory, accepts binary data as input and processes data according to the instructions and provides result as output.

(2) The electronic logic circuits in microprocessor are capable of performing various computing functions and making decisions to change the sequence of program execution.

(3) Microprocessor can also be viewed as an integrated circuit, that contains processing capabilities of large computers.

(4) A microprocessor can be roughly divided into three parts:



1. Arithmetic and logic unit (ALU)
2. Registers
3. Control unit

A.L.U is arithmetic and logic unit, where arithmetical and logical operations are carried out. Registers are primarily used to store data temporarily during execution of program. Control unit provides timing and control signals to the whole system. It also controls flow of data.

(5) **The functions of microprocessor are given below:**

(a) To fetch, decode and execute instructions.

(b) To transfer data from one block to another block or from one block to I/O lines.

(c) To give proper response to different externally produced interrupts according to their priority.

(d) To provide control and timing signals to the whole system according to the instructions.

Topic:Introduction to Microprocessors and Organization of 8085 ; Sub-topic:Functions_Target-2017_XII–HSC Board Exam __Computer Science-II

(B)

(a) (i) **Instruction decoder :**

(1) This interprets the content of instruction register and determines exact steps to be followed in executing the entire instruction.

(2) It directs the control section accordingly.

(ii) **General Purpose Register:**

The General Purpose Register are

(a) Register-B - 8 Bit

(b) Register-C - 8 Bit

(c) Register-D - 8 Bit

(d) Register-E - 8 Bit

(e) Register-H - 8 Bit
(f) Register-L - 8 Bit
(g) Temporary Register - 8 Bit
(h) Flag/Status Register - 8 Bit

(iii) **Data/Address Buffer:**

The content stored in the stack pointer and program counter is loaded into the address buffer and address-data buffer to communicate with the CPU. The memory and I/O chips are connected to these buses; the CPU can exchange the desired data with the memory and I/O

(iv) **Status Register:**

(a) Status register is called as flags, which consist of flip- flops that are set or reset according to data conditions in accumulator.

(b) The generic MPU has two flags : Zero flag and Carry flag.

Topic:Introduction to Microprocessors and Organization of 8085 ; Sub-topic:Functions of Block_Target-2017_XII–HSC Board Exam __Computer Science-II

(b) (1) The pathways through which individual systems are connected in a network are called as transmission media.

(2) Transmission media makes transmission of electronic signals possible from one computer to another. These electronic signals are nothing but binary pulse (I/O).

Characteristics of Transmission Media:

(1) Bandwidth

(i) Bandwidth is the measure of the capacity of a medium to transmit data.

(ii) Data transmission rates is number of bits transmitted per second.

(iii) Bandwidth of a cable depends on cable length.

(2) **Band usage**

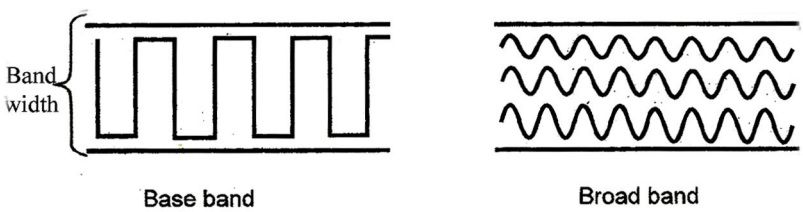
(i) The bandwidth is shared so that maximum usage is obtained.

(ii) There are two transmission modes, base band and broad band transmissions.

(iii) Base band devotes the entire capacity of the medium to one communication channel.

(iv) Broad band enables two or more communication channels to share the bandwidth of communication medium.

(v) The base band and broad band transmission modes are shown in following figure



(3) **Attenuation**

(i) Attenuation is a measure of how much a signal weakens as it travels through a medium.

(ii) As signals pass through the medium, part of the signal is absorbed and makes the signal weak.

(4) **Immunity from electromagnetic interference (EMI)**

(i) Electromagnetic interference consist of outside electromagnetic noise that distorts the signal in a medium.

(ii) EMI is interfering the signals and makes difficult for computers to decode the signal.

(5) **Cost of media**

(i) One major factor in purchase decision of any networking component is its cost.

(ii) For a new fast technology, cost is also more expensive.

(iii) Decision depends upon application and standard of the resources.

(iv) Therefore, the network designer must settle for something, which is cheaper and robust.

(6) **Installation requirement**

(i) Some transmission media requires skilled labour to install. This increases cost of network and it may cause certain delay.

(ii) Before installation we need to prepare actual physical layout of network.

Topic:Networking Technology; Sub-topic:Transmission Media_Target-2017_XII–HSC Board Exam __Computer Science-II

5. (a)

Label	Mnemonics	Comments
	LXI H, 44FFH	; Load HL pair with 44FFH
	LXI D, 4600H	; starting address of destination
	MOV C, M	; Move count in Reg. C
	INX H	; Increment HL Pair
LOOP :	MOV A, M	; Transfer memory to Acc.
	STAX D	; Store Acc. to new location
	INX H	; Increment HL pair
	INX D	; Increment DE pair
	DCR C	; Decrement count
	JNZ LOOP	; Jump to LOOP if count is not zero
	RST 1.0	; Restart

Topic: Instruction Set and Programming of 8085_Target-2017_XII–HSC Board Exam __Computer Science-II

(b)

Label	Mnemonics	Comments
START :	LXI H, 4500	; Initialize HL pair to memory address 4500 H
	MVI B, 00H	; Initialize register to store MSB of sum
	MOV A, M	; Move first number in accumulator
	INX H	; Get address of next number
	ADD M	; Add next number to accumulator
	DAA	; Decimal adjust accumulator
	JNC L1	; In carry ? No, jump to label L1
	INR B	; Increment register B
L1 :	INX H	; Increment HL pair by 1
	MOV M, A	; Store LSB of Sum in memory
	MOV A, B	; Move MSB of Sum in accumulator
	INX H	; Increment HL pair by 1
	MOV M, A	; Store MSB of Sum in memory
END :	RST 1.0	; Restart

Topic: Instruction Set and Programming of 8085_Target-2017_XII–HSC Board Exam __Computer Science-II

(c)

Label	Mnemonics	Comments
	LXI H, 4500	; Initialize HL pair with starting address
	MVI A, 09H	; A = 09H
	MVI B, 05H	; Count in reg. B
UP :	MOV M, A	; Copy data 09H in 4500 H
	INX H	; Increment HL pair
	INR A	; Increment content in A by 1
	DCR B	; Decrement count
	JNZ UP	; Jump to label UP if count in not zero
	RST 1.0	; Restart

Topic: Instruction Set and Programming of 8085_Target-2017_XII–HSC Board Exam __Computer Science-II

OR

5.

(a)

Label	Mnemonics	Comments
	LXI, 4500 H	; Set H-L pointer to 4500 H
	MOV A, M	; take no. in accumulator
	RRC	; with 4 RRC instructions
	RRC	; Interchange the digits of the no.
	RRC	
	RRC	
	INX H	; Increment HL pair by 1
	MOV M, A	; store the exchanged no. in 4501 H
	RST 1.0	; Restart

Topic: Instruction Set and Programming of 8085_Target-2017_XII–HSC Board Exam __Computer Science-II

(b)

Label	Mnemonics	Comments
	LXI H, 44FFH	; Set H-L pointer to 44FFH
	MOV C, M	; Set count = [44FF]
	MVI A, D9H	; Set [Acc.] = D9 H
Loop :	INX H	; [H-L] = [H-L] + 1
	CMP M	; Is [M-L] = D9H ?
	JZ escape	; escape, if [M-L] = D9 H
	DCR C	; count = count - 1
	JNZ Loop	; repeat, if count $\neq$ 0
	LXI H, 5000 H	; Set H-L pair to 5000 if number is not found
escape :	RST 1.0	; Restart

Topic: Instruction Set and Programming of 8085_Target-2017_XII–HSC Board Exam __Computer Science-II

(c)

Label	Mnemonics	Comments
	LXI H, 4500 H	; Set HL pointer to 4500 H
	MOV C, M	; Get count in register C
	MVI A, 00H	; Make LSB's of sum = 00
	MOV B, A	; Make MSB's of sum = 00
LOOP :	INX H	; Set HL to point num in series
	ADD M	; Previous No. + Next No.
	JNC AHEAD	; Is carry ? No, goto AHEAD
	INR B	; Yes, add carry to MSB's of sum
AHEAD :	DCR C	; Decrement count
	JNZ LOOP	; Is count = 0 ? No, jump to LOOP
	STA 4600 H	; Store LSB's of the sum to 4600 H
	MOV A, B	; Get MSB's of sum in accumulator
	STA 4601 H	; Store MSBs
	RST 1.0	; Restart

Topic: Instruction Set and Programming of 8085_Target-2017_XII–HSC Board Exam __Computer Science-II