XII HSC - BOARD - MARCH - 2016

Date: 14.03.2016

COMPUTER SCIENCE - II (D-9)
SOLUTIONS

1. (A)

(a) (ii) 8051 **[1 Mark]**

(b) (iv) MOV A, B **[1 Mark]**

(c) (iii) REPEATER **[1 Mark]**

(d) (ii) ADI **[1 Mark]**

1. (B)

(a)

Microprocessor 8085	Microcontroller 8051
a) It is an 8-bit μp	a) It is a 8-bit microcontroller.
b) Address bus is 16-bit, hence can access 64KB memory.	b) Address bus is 16-bit, hence can access 64KB memory
c) It provides seven 8-bit registers –A, B, H…	c) It provides 34 –8 bit registers –A, Band 32 general purpose registers.
d) 8-bit of data bus but ports are not available.	d) It has four ports P0-P3 for I/O
e) Flag register is 8-bit and contains Five flags.	e) Flag register is 8-bit and contains Nine flags.
f) Peripheral chips are required	f) Peripheral chips are not required

[3 Mark]

Topic:_Microcontroller 8051; XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

(b) (i) **Accumulator :**

(a) Accumulator is 8-bit main register in 8085, used to perform the arithmetical and logical operations. In such operations, one of the operand is always stored in accumulator.

(b) It can be used as both primary source and destination register. The final result of operation is also stored in accumulator.

(c) All data transfer between the CPU and I/O devices are performed through accumulator.

(d) Many memory reference instructions move data between the accumulator and memory.

(iii) **Program counter :**

(a) The program counter is 16-bit register acting as a pointer to next executable instruction.

(b) It always contains the 16-bit address of the memory location where next executable

instruction is stored.

(c) The microprocessor uses this register to sequence the execution of instruction.

(d) The PC is autoincremented after a particular instruction has been fetched by the MPU.

(iii) **Stack pointer (SP) :**

(a) Stack pointer is a 16-bit register, which contains the address of stack top. i.e. the memory address of last byte entered in stack.

(b) With the help of incrementer/ decrementer, the stack pointer is decremented each time data is pushed onto stack and incremented each time data is popped off the stack. **[3 Marks]**

Topic:Instruction set of 8085; Sub-topic: Instruction_XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

(c) (1) Computers store digital data, while telephone lines can only transfer analog data. If a computer is to be connected to internet through telephone, then it must convert digital data to analog data before transmitting the computer signals.

(2) Converting one signal form to antoher form is called modulation and reconverting it to original form is called as demodulation.

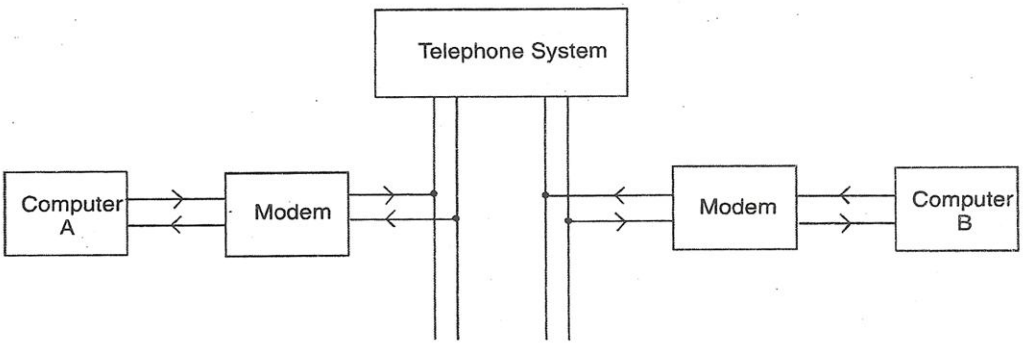
(3) Modern is modulator/demoduator. Modern is used to connect computer to internet. Moderns convert digital data to analog data and vice-a-versa.

(4) They have two advantages:

(a) Modem allows higher speed of transmission on any given analog line.

(b) Modern reduce effect of noise and distortion.

(5) The function of modem is described by following figure.



(6) Modems are classified into two categories according to transmission method.

(a) Asynchronous modems.

(b) Synchronous modems

(a) Asynchronous modems

(i) In asynchronous modems, transmission dock is not used for synchronisation. Instead it uses, bit synchronisation.

(ii) Here each frame begins with a start bit that enables the receiving device to adjust to the timing of transmitted signal.

(iii) Messages are kept short.

(iv) It is used to transmit character data.

(v) Asynchronous transmission is simple, inexpensive technology. It is used for PC to PC communication.

(b) Synchronous modems

(i) Synchronous modes uses clocks on transmitting and receiving devices.

(ii) It uses a 'sync' signal, which is a bit pattern and can be easily recognised by the receiver.
(iii) A wide variety of data types can be transmitted.
(iv) A long series of bits can also be transmitted. **[3 Marks]**

Topic:Networking Technology; Sub-topic: Modem_XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

2. (A)

(a) (1) HLDA :

(a) It is signal for HOLD ACKNOWLEDGEMENT.

(b) A HLDA output indicates to a peripheral that a HOLD request has been received and that the microprocessor will relinquish control of buses in the next clock cycle.

(c) After the removal of HOLD request, HLDA goes low.

(2) SID :

(a) Serial input data. It is a data line for serial input.

(b) For serial data transmission SID pin is used. For this type of transmission RIM and SIM instructions are used.

(3) READY :

(a) It is a input signal used by the microprocessor to sense whether a peripheral is ready to transfer data or not.

(b) This signal is used to delay the microprocessor until a slow responding peripheral is ready to send or accept data.

(c) If READY is high, the peripheral is ready. If it is low, the microprocessor waits for an integral number of clock cycles until it goes high.

(d) It is used to synchronize slower peripheral to faster microprocessor. **[3 Marks]**

Topic:Introduction to microprocessors and org. of 8085; Sub-topic: Pins_;XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

(b) 80386 :

(1) The INTEL's 80386 is a 32-bit microprocessor introduced in 1985.

(2) 80386 is a logical extension of 80286. It is more highly pipelined.

(3) The instruction set of 80386 is a superset of other members of 8086 family.

(4) It has 32-bit data bus and 32-bit nonmultiplexed address bus. It can address a physical memory of 2^{32} i.e. 4 Gbytes. The 80386 memory mangement allows it to address 2^{46} or 64 Tbytes.

(5) The 386 can be operated in one of the following memory management modes:

(a) Paged mode

(b) Non- paged mode.

(6) When operated in paged mode, the 386 switches the paging unit then after the segment unit. The paging unit allows memory pages of 4 KB each to be swapped in and out from disk. In non - paged mode, memory mangement unit operates very similar to the 286.

(7) Virtual addresses are represented with selected components and an offset component as they are with 80286.

(IV) 80486 :

(a) Intel's 80486 is a 32-bit microprocessor. It was introduced in 1989.

(b) It has 32-bit address bus and 32-bit data bus.

(3) The 486 is basically a large integral circuit which contains a fast built-in, a math coprocessor, a memory mangement unit (M.M.U), and an 8 kbyte cache memory.

(4) 80486 has DX and SX versions.

(5) All 486 processor have 32-bit data bus. SX version does not have on chip- numeric coprocessor.

(6) The 486 achieves its high speed operation from its faster clock speeds, internal pipe lined architecture and the use of reduced instruction set computing (RISC) to speed up the internal microcode.

(7) 486 also has 486 DX2 and 486 DX4 versions, with double and triple clock speed.

(V) Pentium or 80586 :

(1) Pentium is a 64 bit microprocessor, introduced in 1993.

(2) It has 64 bit data bus and 32-bit address bus. The use of super scalar architecture incorporates a dual- pipe lined processor, which lets and Pentium process more than one instruction per clock cycle.

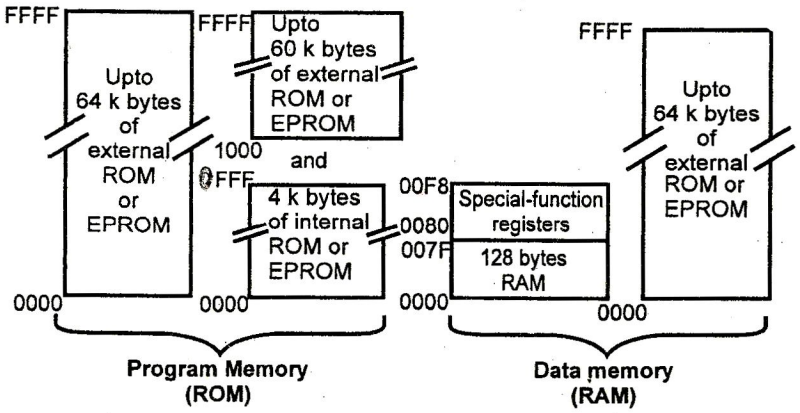
(3) The addition both of data and code caches on chip is also a feature designed to improve processing speed.

(4) A new advanced computing technique used in Pentium is called the brach prediction, the Pentium makes an educated guess where the next instruction following a conditional instruction will be. This prevents instruction cache from running dry during conditional instructions.

(5) The pentium has 64-bit data bus. This means that it can perform data transfers with an external device twice as fast as a processor with a 32 bit data bus. **[3 Mark]**

Topic:Introduction to intel X-86 family; Sub-topic: Members of X-86 family_XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

(c)



[3 Marks]

Topic:Introduction to Microcontroller; Sub-topic: Memory register map_;XII–HSC Board Exam _ Target-2016_Comp. Sci. II_NKcs Mam

2. (B)

(a)

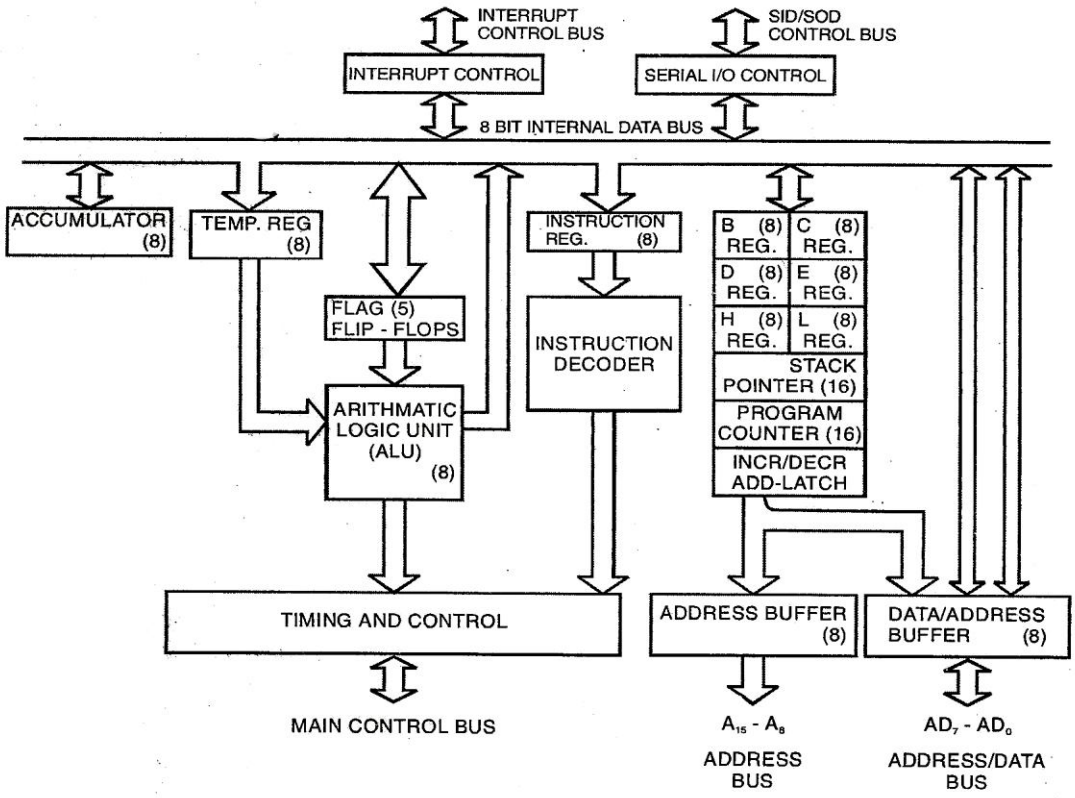


Fig. (1.5) Internal Block Diagram of 8085

[4 Marks]

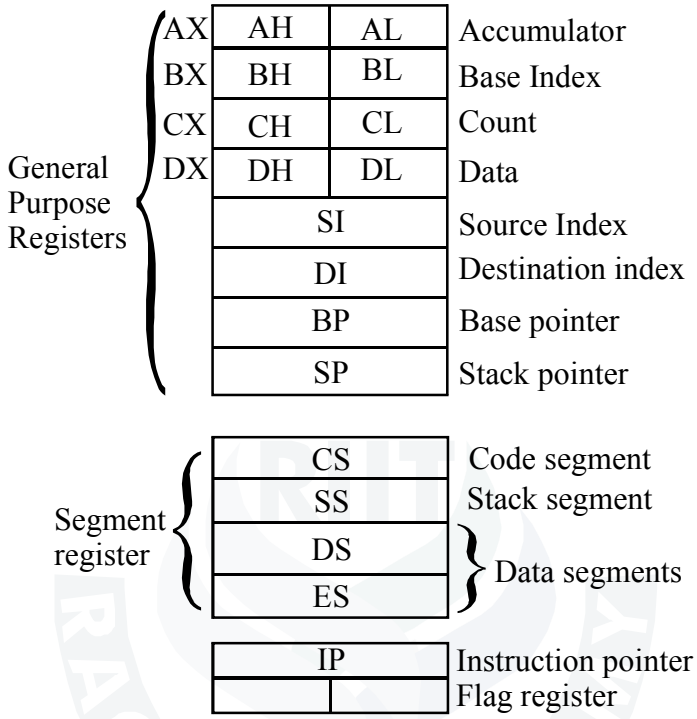
Topic:Introduction to microprocessors and org. of 8085; Sub-topic: internal block of 8085_;XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

(b) 16-bit version of X-86 Family :

(1) The 8088 and 8086 defines basic programming model for X-86 family.

(2) The 16-bit version for programming model is used in 16-bit microprocessor of X-86 family *i.e.,* in 8088, 8086 and 80286.

(3) The 16 - bit version of programming model of X- 86 family is shown in the following figure.



Programming model of 16-bit version of X-86 family

(5) As shown in above figure the programming model of 16-bit version of X-86 family consists of three register groups.

(6) The first contains 8-general purpose registers called A, B,C,D,SI, DI, SP and BP registers. Al, BL,..... indicates lower bytes and AH, BH, ... indicates higher bytes. The full 16-bit registers are referred as AX, BX, CX and DX, where X stands for extended SI, DI, BP, SP registers are always treated as 16-bit registers. These are pointer register because they are used to point locations within a segment.

(7) The second group of registers is the segement group of registers. This group consists of code segment, stack segment and two data segment registers. Operation with external memory. Address compulations and data movements are performed here.

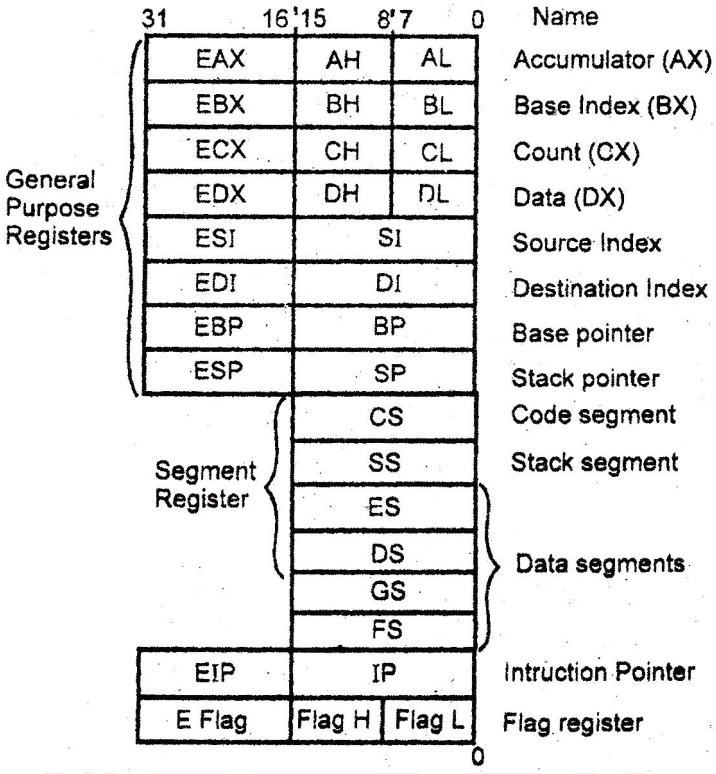
(8) The third group of registers consists of instruction pointer (IP) and fla register.

32-bit version of X-86 Family :

(1) The 8088 and 8086 defines the base programming model for the entire X-86 family of advanced microprocessors.

(2) The newer members of X- 86 family have greater computing power because they are faster, they use 32-bit registers instead of 16-bit register and they have advanced addressing techniques.

(3) Following figure show programming model for 32-bit version of X-86 family used in 32 bit microprocessor family i.e. in 386,486 and pentium.



(4) The programming model of 32-bit version of X-86 family consists of 3 register groups.

(5) The first group contains eight general purpose registers called EX, EBX, ECX, EDX, ESI, EDI, ESP and EBP registers. Where E tells us that these registers have extented length. Each register can be addressed in 1,8,16 or 32- bit models. These registers are used to store data during computations.

(6) The second group of resisters is the segment group. This group consists of code segment, stack segment and four data segment registers. The data segment registers are DS, ES, FS and GS. These registers manage operation with external memory. Address computations and data movements are performed here.

(7) The third set of registers consists of Instruction Pointer (I.P.) and flag register. **[4 Marks]**

Topic:Introduction to microprocessors and org. of 8085; Sub-topic: internal block of 8085_;XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

3. (A)

(a) (i) **Direct addressing mode :**

(a) In direct addressing, the address appears after opcode of instruction in program memory.

(b) The address of operand is specified within the instruction.

(c) The instructions using direct addressing mode are three byte instructions. Byte 1 is opcode of instruction, Byte 2 is lower order address and Byte 3 is high order address.

(d) For e.g. LDA C060 H

i.e. This instruction loads accumulator with content of memory location C060 H.

(ii) **Register addressing mode :**

(a) In register addressing mode, the source operands are general purpose registers whose name is specified within the instruction.

(b) These instruction are single byte instructions.

(c) All actions occur within the CPU.

(d) For e.g. MOV A,B.

i.e. This instruction transfers the content of register B to accumulator without modifying content of B.

(iii) **Immediate addressing mode :**

(a) In Immediate addressing the data appears immediately after opcode of instruction in program memory.

(b) In these instructions the actual data is specified within the instruction.

(c) These operations are specified with either 2 or 3 byte instructions.

(d) For e.g. ADI 05H

i.e. this instruction adds immediate data 05 H to the content of accumulator. The result is stored in accumulator. **[3 Marks]**

Topic:Introduction to microprocessors and org. of 8085; Sub-topic:Addressing mode_;XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

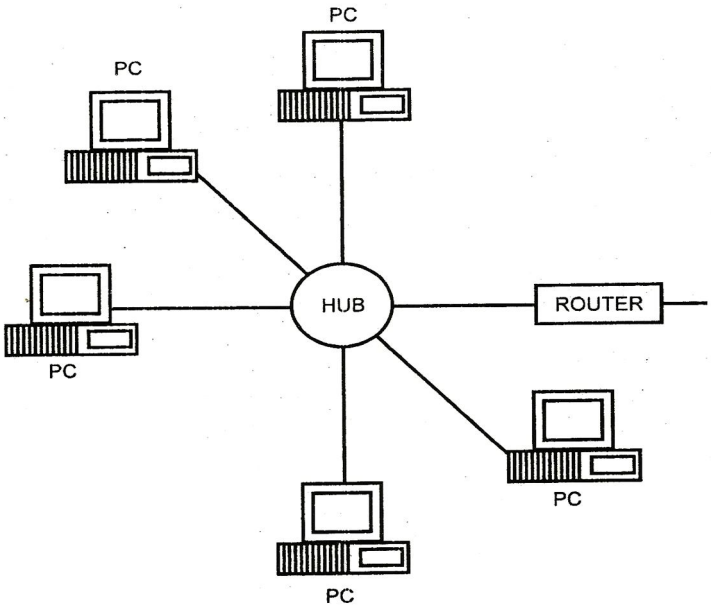
(b) (i) STAR Topology:

(1) In a STAR topology all the workstations are connected to central hub.

(2) The hub receives signal from a workstation and routes it to the proper destination.

(3) STAR physical topology is often implemented to implement BUS or RING logical topology.

(4) A STAR topology is shown in following figure:



*** Advantages:**

(1) Adding a new workstation is easier than that in BUS or RING topology.

(2) The control is centralised due to use of hub

*** Disadvntages:**

(1) Hub failure affects all users.

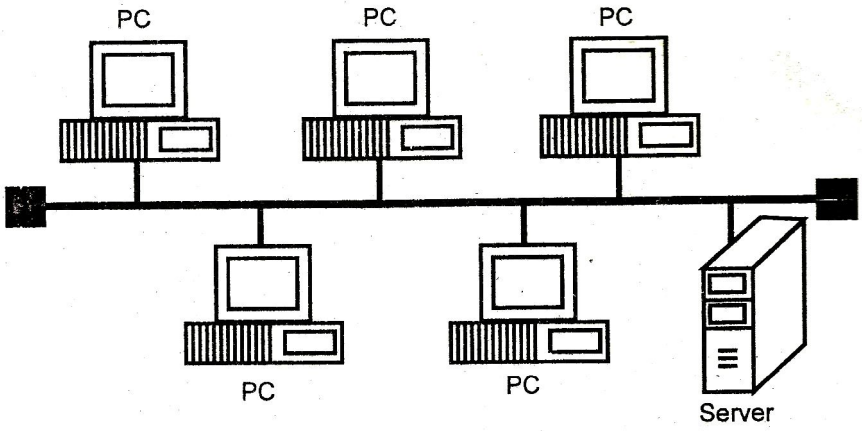
(2) Hubs are slightly expensive.

(3) STAR topology requires more cabeling than BUS or RING topology. Hence, it costs more.

(ii) BUS Topology :

(1) In a BUS physical topology, all the devices are connected to a common shared cable, called as backbone of the network.

(2) A BUS physical topology is shown in following figure :



(3) The bus is available for each node to send its data to each and every computer node.

***Advantages:**

(1) The bus system is much faster.

(2) The bus topology can be extended with sub branches to form another topology.

(3) Breakdown of any failure node does not affect other node's communication.

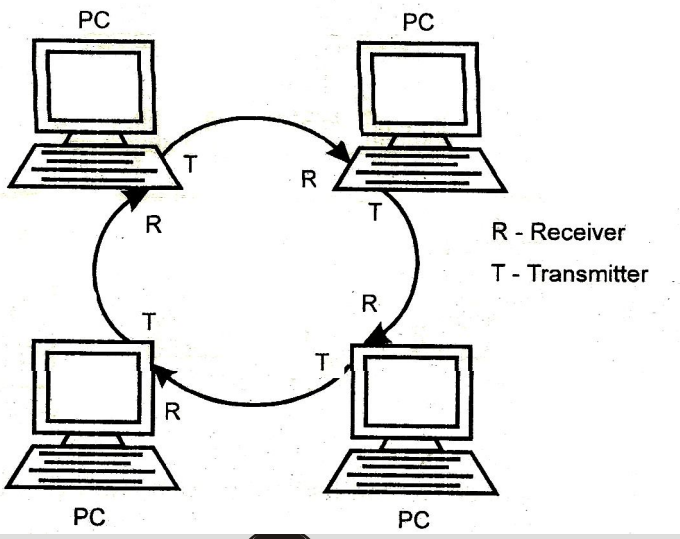
(4) Bus topology is widely used in LAN network.

(iii) RING Topology:

(1) RING topologies are wired in a circle. Each node is connected to its neighbours on either side, and the data transmits along the ring in one direction only.

(2) Each device incorporates a receiver and a transmitter and serves as a repeater that passes the signal onto the next device in the ring.

(3) The RING topology is as shown in following figure:



(4) RING topologies are suited for networks that uses token passing access methods. The token passes around the ring, and the only node that holds the token can transmit data.

(5) This topology is always implemented as a logical topology.
e.g. In token ring network, the topology is physically a STAR topology. But logical topology is RING topology.

(6) The commonly used implementation for RING topology is token ring at 4-16 MBPS.

***Advantages:**

(1) Cable failure affects limited users.

(2) Each node has equal access speed to the ring.

(3) Equal access for all users.

***Disadvantages:**

(1) Costly wiring is required for RING topology.

(2) Expensive adapter cards.

(3) Difficult connections. **[3 Marks]**

Topic:Networking Technology; Sub-Topic:Topology_XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

(c)

WAN	LAN
a) A wan (Wide Area Network) is the interconnection of LAN or MAN can be located entirely within a state, country or around the world.	A LAN (Local Area Network) is a group of computers interconnected within a small area such as room, building or a campus.
b) Data transfer rate is comparatively slower such as is Kbits/ sec. 10 million bits per second.	Data transfer speed is comparatively high such as thousand bits per second.
c) In WAN, links may be established by using telephone cable or microwave towers or satellite.	Co- axial cables are generally used to connect the computer and other devices.
d) In this network, shortcircuit errors, noise errors, atmospheric errors are higher than any other networks.	Due to short distance, short circuit errors or other noise errors are minimum.
e) For example : Pager.	For example : A computer lab in a college.

[3 Marks]

Topic:Networking Technology; Sub-Topic:Network types_XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

3. (B)

(a) (1) An interrupt is a subroutine called, initiated by external device through hardware (hardware interrupt) or microprocessor itself (software interrupt).

(2) An interrupt can also be viewed as a signal, which suspends the normal sequence of microprocessor and then microprocessor gives service to that device which has given the signal.
After completing the service, microprocessor again returns to the main program.

(3) Hardware interrupts are used to handle asynchronous events. These interrupts are requested by external device.

(4) After execution of these interrupts program counter is not incremented. The microprocessor executes either interrupt acknowledge cycle or ideal machine cycle to acknowledge this interrupt.

(5) These interrupts may be non- maskable or maskable.

(6) They have lower priority than any software interrupt.

8085 provides 5 hardware interrupts:

(i) TRAP (ii) RST 7.5 (ii) RST 6.5 (iv) RST 5.5 (v) INTR

(1) These interrupts are vectored interrupts. It means that when these interrupts are given , it is directed (or vectored) to transfer the control to specific memory location given by

TRAP $= 4.5 \times 8 = 0024$ H RST $7.5 = 7.5 \times 8 = 003$C H

RST $6.5 = 6.5 \times 8 = 0034$ H RST $5.5 = 5.5 \times 8 = 002$C H

(2) Among these interrupts, TRAP is non- maskable interrupt which can not be disabled. But the other four interrupts are maskable interrupts, which can be disabled.

(3) The TRAP has highest priority and the INTR has lowest priority among the hardware interrupts. The hardware interrupts in descending order of priority are listed below:

(i) TRAP - **highest priority** (ii) RST 7.5 (iii) RST 6.5

(iv) RST 5.5 (v) INTR - **lowest priority.** **[4 Marks]**

Topic:Introduction to microprocessors and Org. of 8085; Sub-topic: Interrupts;XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

(b) (i) Dual pipelining :

The use of super scalar architecture incorporates a dual pipelining in Pentium processor, which lets Pentium to process more than one instruction per clock and achieve a high level of performance.

(ii) Prefetching: Out of syllabus

(iii) Branch prediction:

(i) The advantage of branch prediction is that, using branch prediction, it makes an, intelligent guess of the next conditional instruction.

(ii) This prevents the instruction cache from running dry during conditional instruction.

(iv) Internal Data Bus

(i) Pentium has 64 bit data bus which allows higher speed of data transfer to it.

(ii) The data transfer speed of Pentium is twice as fast as a processor with 32- bit data bus.

[4 Marks]

Topic:Introduction to X-86 Family;Sub-topic-Pentium Processor;XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

4. (A)

(a) (1) A protocol is defined as an agreement between communication particle for how communication should be proceed.

OR

Protocols are rules by which computers communicates i.e. protocol is set of rules and formats for sending and receiving data.

(2) Internet protocol are called TCP/IP (Transmission Control Protocol/Internet Protocol) protocols. This protocol do not belong any one company and technology is available to everybody.

(3) TCP/IP protocol use three types of addresses for network addressing

(a) Hardware or physical address is used by the data link and physical layers.

(b) Internet protocol address provides logical node identification. This address is unique address assigned by administratory expressed in four parts dotted notation.

e.g. 123.144.131.21

(c) Logical node names are easier to remember than an IP address. **[3 Marks]**

Topic:Networking Technology; Sub-topic: Protocol_XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

(b) (1) The light wave can be efficiently conducted through transparent glass fiber cables known as optic fiber cables.

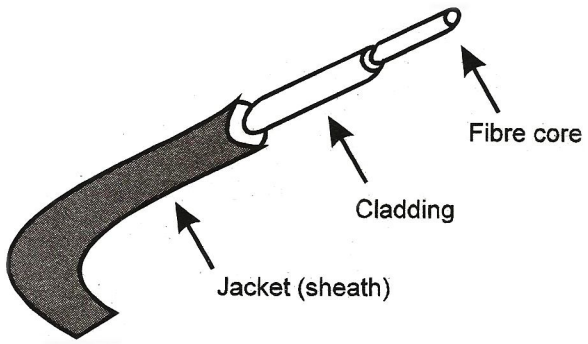
(2) The centre conductor of this cable is a fibre that consists of highly refined glass or plastic.

(3) It is designed to transmit light signals with little loss.

(4) The fibre is coated with cladding or gel that reflects signals back into fibre to reduce signal loss.

A plastic sheet protects the fibre from damage.

(e) The fibre optic cable is shown in following figure.



(f) The fibre optic cable is used in optical transmission system.

(g) This cable have extremely high bandwidth. It has zero sensitivity to EMI and runs over several kilometers.

(h) The characteristics of fibre optic cable are given below

(i) **Cost** : The cost of fibre optic cable is more than that of co-axial cable and Twisted pair cable.

(ii) **Installation** : Fibre optic cable requires skilled installation. Every cable has minimum bend radius. They may get damaged if bent sharply Fibre optic cable can not be stretched.

(iii) **Capacity** : Fibre optic cable supports high data rates (upto 2,00,000 MBPS), even with long run cables. Fibre optic cable can transmit 100 MBPS for several kilometer.

(iv) **Attenuation** : Attenuation for fibre optic cable is much lower than co-axial cable and twisted pair cable. It can run to larger distance.

(v) **EMI** : Fibre optic cable does not use electrical signals to transmit data, therefore they are free from EMI. The data trasfer in fibre optic cable have high security, as it can not be detected by electronic wave dropping equipments. **[3 Marks]**

Topic:Networking technology;Sub-topic: Bounded Media_XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

(c) The microprocessor 8086 has 16-bit register with 9 active flages, which are shown in following figure.

Where,

Cy - Carry flag

P - Parity flag

AC - Auxiliary carry flag

Z - Zero flag

S - Sign flag

TF - Trap flag

IF - Interrupt flag

DF - direction flag

OF - over flow flag

The first five bits are identical to 8085.

In data flag category OF (Overflow) flag is there, rests of the flags are same as 8085 flags.

- OF– Overflow Flag– Used in signed numbers, when the result of signed number is too large, causing MSB to overlfow into the sign bit, this flag is set.
- DF – Direction Flag – Used to control the direction (increment/decrement) of the string operation.
- IF – Interrupt Flag – Used to enable or disable external maskable interrupt requests.
- TF – Trap Flag – Used for single stepping instructions. **[3 Marks]**

Topic:Introduction to X-86 Family; Sub-topic:Flag_ XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

4. (B)

(a) 8051 is a second generation microcontroller.

(1) **8048, 8049, 8050**

(a) Intel's first microcontroller was 8048. The 8048, 8049 and 8050 all have indentical architectures with the exception of memory size.

(b) In each case, the memory doubles. 8048 supports 1K byte of internal memory. 8049 supports 2k bytes of internal memory and 8050 supports 4K bytes of internal memory.

(c) 8048 has 64 bytes internal RAM, including 32 bytes of register/memory location. The 8049 and 8050 have a total of 128 and 256 bytes of RAM respectively.

(d) The microcontrollers are low cost products and hence are very popular.

(2) **8052**

(a) 8052 is a simple expansion of 8051

(b) 8052 has 8K bytes of onboard ROM and 256 bytes of onboard RAM.

(c) 8052 allows programmers to write larger programs and that can use more data.

(d) The cost of 8052 is more than that of 8051.

(e) The 8052 also has one extra 16-bit counter-time. This counter-time gives more flexibility.

(3) **8031 and 8032**

(a) The alternative versions of 8051 and 8052 are 8031 and 8032.

(b) These devices do not have any on board ROM. It may use external ROM for program memory.

(c) These are excellent devices for prototyping and low-volume products.

(4) **8052 AH-BASIC**

(a) Another form of 8052 is 8052 AH-BASIC. This special 8052 has BASIC programming language in ROM.

(b) Using BASIC instructions, a programmer can write instructions for this 8052 rather than assembly language. **[4 Marks]**

Topic:Introduction to Microcontroller; Sub-topic:Microcontroller types_XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

(b) (1) Ethernet is a local area network technology, with networks tradionally operation within single building.

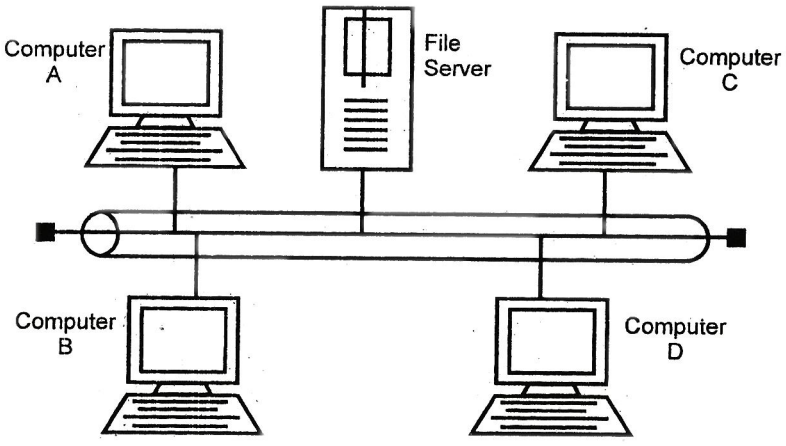
(2) Atmost, Ethernet devices can have a few hundred meters of cable between them. Modern technology allows Ethernet to span upto 10 kms.

(3) Ethernet devices are connected to a common shared medium that provides the path along which the electronic signals will travel. Historically, this medium was co-axial cable. But, now-a-days twisted pair cable or fibre optic cable are also used.

(4) Ethernet network transmit data in small units called **frames.**

(5) Each frame must contain source address as well as destination address, which identifies receipant and sender of message. The address will uniquely indentify node. No two Ethernet devices can have same address.

(6) Ethernet network is as shown in following in figure.



In above figure when computer A sends message to computer C, computer B and D will alsoget the message and check whether the destinations address mathches to its own address or not, it not, it will discard the frame. **[4 Marks]**

Topic:Networking Technology; Sub-topic-Ethernet_;XII–HSC Board Exam _Target-2016_Comp. Sci. II_NKcs Mam

5.

(a)

Label	Mnemonics	Comments
	SUB A	; clear the accumulator
	MOV D, A	; clear the D register
	LXI H, 1050H	; load immediately 1050 to HL pair
	MOV B, M	; move memory to B reg.
	INX H	; increment HL pair
	MOV C, M	; move memory to C reg.
BACK:	ADD B	; add B with accumulator
	JNC NEXT	; jump if not carry to NEXT
	INR D	; increment D reg.
NEXT :	DCR C	; Decrement C reg.
	JNZ BACK	; jump if not zero to BACK
	INX H	; increment HL pair
	MOV M, A	; move accumulator to memory
	INX H	; increment HL pair
	MOV M, D	; move D reg. to memory
	RST 1.0	; Restart

[5 Marks]

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(b)

Label	Mnemonics + Operand	Comment
	LXI H, 1050	; Load content from 1050 to memory
	LXI D, 1070	; Load content from 1070 to D reg.
	MVI C , 0A	; Set counter to 0A H
up :	MOV A, M	; Move content from memory to Acc.
	STAX D	; Store Acc. content to D Reg.
	INX H	; Increment HL pair by 1
	INX D	; Increment D pair by 1
	DCR C	; Decrement counter
	JNZ :up	; Jump If not zero to label up
	RST 1.0	; Restart

[5 Marks]

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(c)

Label	Mnemonics + Operand	Comment
	LHLD C000	;Load HL pair from C000 memory location
	DAD H	;Add register pair to HL pair
	DAD H	;Add register pair to HL pair
	DAD H	;Add register pair to HL pair
	SHLD BC	;Store HL pair to BC register pair
	RST 1.0	; Restart

[5 Marks]

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OR

5.

(a)

Label	Mnemonics + Operand	Comment
	LXI H,1050 H	;Initialise HL pair to memory address 1050 H
	MVI B, 00H	:Initialise register to store MSB of sum
	MOV A, M	:Move first number in accumulator
	INX H	;Get address of next number
	ADD M	;Add next number to accumulator
	DAA	;Decimal adjust accumulator
	JNC L1	;Is Carry ? No, jump to label L1
	INR B	;Increment register B
L1:	INX H	;Increment HL pair by 1
	MOV M, A	;Store LSB of Sum in memory
	MOV A, B	;Move MSB of Sum in accumulator
	INX H	;Increment HL pair by
	MOV M, A	;Store MSB of Sum in memory
	RST 1.0	;Restart

[5 Marks]

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(b) The accumulator value is $B7_H$ and B register value is $A5_H$

(i) ADI 05

Add immediately with 05_H
Before execution [A] = $B7_H$ = 1 0 1 1 0 1 1 1
Instruction - ADI 05
After execution [A] = 1 0 1 1 1 1 0 0 **[1 Mark]**

(ii) CMP B

Compare B with accumulator
Before execution [A] = $B7_H$ = 1 0 1 1 0 1 1 1
Before execution [B] = $A5_H$ = 1 0 1 0 0 1 0 1
Instruction - CMP B
Condition:
(a) If [A] < [B] then Carry flag is set.
(b) If [A] = [B] then Zero flag is set.
(c) If [A] > [B] then both Carry and Zero flags are reset. **[1 Mark]**

(iii) CMA

Complement the accumulator
Befor execution [A] = B7H = 1 0 1 1 0 1 1 1
Instruction - CMA
After execution : 48_H = 0 1 0 0 1 0 0 0 **[1 Mark]**

(iv) XRA B

Exclusive OR with accumulator
Before execution [A] = $B7_H$ = 1 0 1 1 0 1 1 1
Before execution [B] = $A5_H$ = 1 0 1 0 0 1 0 1
After execution : 12_H = 0 0 0 1 0 0 1 0 **[1 Mark]**

(v) ORA B

Logical OR with B

Before execution [A] = $B7_H$ = 1 0 1 1 0 1 1 1

Before execution [B] = $A5_H$ = 1 0 1 0 0 1 0 1

After execution : $B7_H$ = 1 0 1 1 0 1 1 1 **[1 Mark]**

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(c)

Label	Mnemonics + Operand	Comment
	LDA 1051	;Initialise HL pair to memory address 1051 H
	INR A	;Increment accumulator by 1
	INR A	;Increment accumulator by 1
	LDA 1053	;Load accumulator from 1053 memory location
	INR A	;Increment accumulator by 1
	INR A	;Increment accumulator by 1
	LDA 1055	;Load accumulator from 1055 memory location
	INR A	;Increment accumulator by 1
	INR A	;Increment accumulator by 1
	LDA 1057	;Load accumulator from 1057 memory location
	INR A	;Increment accumulator by 1
	INR A	;Increment accumulator by 1
	LDA 1059	;Load accumulator from 1059 memory location
	INR A	;Increment accumulator by 1
	INR A	;Increment accumulator by 1
	RST 1.0	;Restart

[5 Marks]

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