2003 CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING(C-DAC) M.C.A

END-TERM EXAMINATION
SECOND SEMESTER [MCA] –MAY 2003
COMPUTER SYSTEM ARCHITECTURE

Paper Code: MCA-106
Time: 3 Hours
Marks: 60

Q. 1 (a) What is De-Multiplexer? How can you make decoder to function as a Demultiplexes?

Show this by a block diagram and truth table. 5

(b) Given a 32 x 8 ROM chip with an enable input, show the external connection necessary to construct 128 x 8 ROM with four chips and a decoder. 7

Q. 2 (a) If we need to link 16 registers to a common bus, when each register is 32-bit then, 6

(i) How many multiplexer will be required?
(ii) How many input lines are required for each multiplexer? This should also include adequate number of selection lines.

(b) Register A holds the 8-bit binary 11011001, determine the B operand and the logic micro-operation to be performed in order to change the value in A to
(i) 01101101 (ii) 11111101. 6

Q. 3 (a) With the help of flow chart, explain the sequence of steps for an instruction cycle. How does an interrupt change the sequence of events? 6

(b) Give the schematic diagram of a micro program sequence and briefly explain functions of its different components. 6

Q. 4 (a) Convert the following numerical arithmetic expressions into reverse polish notation and show the stock operations for evaluating the results. 6
(3+4) [10 (2+6) + 8]

(b) What do you understand by “Reduced instruction set computer” (RISC), How are they differ from CISC. 3

(c) What is difference between direct addressing mode and indexed addressing mode instruction. 3

Q. 5 (a) Discuss the application of pipelines, illustrate through a system having 4

segment instruction pipelines. Also discuss what is speed up in a pipeline architecture. 5

(b) Calculate the speed up in case of a computer with four floating-point pipeline processors. Each processor uses a cycle time of 40 µs. Total number of floating point operation to be made is 400. 5

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Note: Attempt any five questions.

(c) Differentiate between supercomputer & Multi-computers 2

Q. 6 (a) Explain Booth's algorithm for multiplication. Give the schematic diagram of the hardware needed to implement Booth's algorithm. Depict the algorithm using the hardware through a flow chart's what happens when there is an overflow?

6

(b) A 48 bit computer stores floating point number is sign-magnitude form with 12 bits for exponent (including sign bit). Find the range of numbers that can be represented on this computer. 6

Q. 7 (a) What is I/O processor and what are its functions & advantages? Also discuss how I/O interrupts make more efficient use of CPU. 6

(b) In case of Direct-mapping cache & Fully associated Cache and considering their merits discuss / answer the following; 6

(i) rank these in terms of hardware complexity & implementation cost.
(ii) With each cache organization, what is the effect of block-mapping policies on the hit-issue ratio.

Q. 8 Write short note on any three:- 3 x 4

(a) Hardwired control and micro-program control
(b) Virtual memory concept.
(c) Overlapped Register windows
(d) Arithmetic pipeline
(e) SIMD array processor.