ANSWER KEY

FIRST YEAR HIGHER SECONDARY EXAMINATION ~~MARCH~~ JUNE 2022

PART-I/II/III

SUBJECT: ELECTRONICS

CODE NO: FY 31 VERSION: A

60 SCORES 2 HOURS

Qn. No	Sub Qns	Answer Key/Value Points	Score	Total Score
1		c	1	1
2		c $\frac{V_m}{\sqrt{2}}$	1	1
3		d 0.7 eV	1	1
4		c 0.7 V	1	1
5		c 0.8	1	1
6		a Solar Cell	1	1
7		a V_m	1	1
8		b CE Configuration	1	1
9		d $\frac{1}{2\pi\sqrt{LC}}$	1	1
10		d 111	1	1

Qn. No	Sub Qns	Answer Key/Value Points	Score	Total Score
11		Passive – Capacitor, Inductor, resistor Active – Transistor, Diode, IC	2	2
12		Definition of doping	2	2
13		The potential barrier near by the PN junction which prevents further movement of charge carriers across the junction	2	2
14		1 Score each for the symbols of NPN and PNP transistors	2	2
15		Symbol – 1 Score Applications – 1 Score	2	2
16		Principle – 1 Score Symbol – 1 Score	2	2

Qn. No	Sub Qns	Answer Key/Value Points	Score	Total Score
17	(a)	$\gamma = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$	1	
	(b)	1.21	1	2
18		Oscillations whose amplitude continuously decreases with time due to losses	2	2
19		$A\beta = 1$ Total phase shift around the loop = 0° or 360°	2	2
20		Brown, Black, Red, Gold	3	3
21		(a) nR — 1 (b) R/n — 2	3	3

Qn. No	Sub Qns	Answer Key/Value Points	Score	Total Score
22		Diagrams — 2 Explanation — 1	3	3
23	(a)	We have to connect the positive terminal of the external supply to the p-type semiconductor of the PN junction.	2	
	(b)	charge carries flow across the junction overcoming the depletion layer	1	3
24	(a)	Diagrams — 2	2	
	(b)	The forward voltage at which the diode starts conducting — 1	1	3

Qn. No	Sub Qns	Answer Key/Value Points	Score	Total Score
25		Physical Size Collector - largest Base - Smallest Emitter - moderate —1 Doping Concentration Emitter - largest Base - Smallest Collector - moderate —2		3
26	(a)	Diagram	2	
	(b)	$A = -\frac{R_F}{R_1}$	1	3
27		Very high input impedence Very high gain Very high bandwidth	3	3
28		Symbol — 1 Truth table — 1 Output expression — 1	3	3

Qn. No	Sub Qns	Answer Key/Value Points	Score	Total Score
29		Circuit diagram	3	3
30				
	(a)	$R_{eff} = R_1 + R_2 + R_3$ — 1		
		$= 100 + 100 + 100 = 300\,\Omega$ — 1	2	
	(b)	$I = \frac{V}{R}$ — 1		
		$= \frac{300}{300} = 1A$ — 1	2	4
31				
	(a)	$V_m = 141\ V$	1	
	(b)	$V_{rms} = \frac{V_m}{\sqrt{2}} = 100\ V$	1	
	(c)	$2\pi f = 314$		
		$f = \frac{314}{2\pi} = 50\ Hz$	2	4

Qn. No	Sub Qns	Answer Key/Value Points	Score	Total Score
32		Circuit diagram — 2 Working — 2	4	4
33	(a)	Circuit diagram	2	
	(b)	Working	2	4
34	(a)	Circuit diagram of Centre-tap full wave rectifier	3	
	(b)	$PIV = V_m$	1	4
35	(a)	Circuit diagram	2	
	(b)	three RC sections provide 360° phase shift	2	4

Qn. No	Sub Qns	Answer Key/Value Points	Score	Total Score
36	(a)	Any basic gate can be derived using either NAND or NOR gate	1	
	(b)	Symbol – 1 Output expression – 1 Truth table – 1	3	4
37	(a)	If both of the inputs are high, the OR gate output will be high but XOR gate output will be low.	2	
	(b)	Symbol – 1 Output expression – 1	2	4