2006 CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING(C-DAC) M.C.A

END-TERM EXAMINATION
SECOND SEMESTER [MCA] – MAY-JUNE 2006
COMPUTER SYSTEM ARCHITECTURE

Paper Code: MCA-106
Time: 3 Hours
Marks: 60

Q. 1 Attempt all parts :- (1 x 10 = 10)
(a) Name a computer machine that combines several instructions into a single instruction.

(b) What is the memory addressing capability of a microprocessor which has 24 address pins?

(c) What is the advantage of having independent set of conditional codes?

(d) What is a monitor program?

(e) What is the head of a disk?

(f) Which industry is the primary user of MICR (Magnetic Inc Character Recognition)?

(g) What prevents RISC pipeline to achieve maximum speed?

(h) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro-operation to be performed in order to change the value of A to 01101101?

(i) Change (A+B)*C in reverse Polish notation?

(j) Determine the number of clocks cycles that it takes to process 200 tasks in a sigsegment pipeline?

Q. 2
(a) What is difference between instruction stream and data stream? (2)

(b) Find out the average access time for a fixed head disk rotating at 300 rpm and contains 10 sectors in a track? (3)

(c) What is the difference between logical shift, circular shift and arithmetic shift. Give suitable examples? (5)

Q. 3
(a) What are the differences between external and internal interrupts? (3)

(b) Define the term Program Status Word. (2)

(c) Design a digital circuit that performs the four logic operations of exclusive-OR, exclusive-NOR, NOR and NAND. Use two selection variables. Show the logic diagram of one typical stage? (5)

Q. 4
(a) What are the differences between Static Memory and Dynamic Memory? (2)

(b) What are four different types of pipelining? (2)

(c) Draw the flowchart for multiplying two floating point numbers? (6)

Q. 5
(a) How a subroutine call is different from branching? (2)

(b) Construct a 5-to-32 line decoder with four 3-to-8-line decoders with enable and one 2-to-4-line decoder? (8)

Q. 6
(a) If the program counter is always one count ahead of the memory location from which the machine code is being fetched, how does the micro-processor change the sequence of program execution with a jump instruction? (3)

(b) Formulate a mapping procedure that provides eight consecutive micro instructions for each routine. The operation code has six bits and the control memory has 2048 words? (3)

(c) Compare the RISC and CISC architecture? (4)

Q. 7
(a) A 36-bit floating point binary number has eight bits plus sign for the exponent and 26 bits plus sign for its mantissa. The mantissa is a normalized fraction. Numbers in the mantissa and exponent are in signed magnitude representation. What are the largest and smallest positive quantities that can be represented, excluding zero? (4)

(b) Explain the difference between hardwired control and micro-programmed control. Is it possible to have a hardwired control associated with a control memory? (6)

Q. 8 Write short notes on any two:- (5 x 2 = 10)
(a) RS 232 C protocol

(b) Associative Memory

(c) IBM PC bus.