# END-TERM EXAMINATION <br> FIRST SEMESTER [MCA] - DECEMBER 2004 

DIGITAL ELECTRONICS
Paper Code: MCA-103
Time: 3 Hours
Marks: 60
Q. 1. (a) Reduce the following:-
(i) $\mathrm{AB}+\mathrm{A}+\mathrm{AB}$
(ii) $(\mathrm{AB}+\mathrm{C})(\mathrm{AC}+\mathrm{BC})+\mathrm{ABC}+\mathrm{AB}$
(b) Give the block diagram of exclusive OR (XOR) gate using 4 NAND gates
only. Write its truth table also.
(c) Subtract (01001)2 from (01000)2 using
(i) 1's Complement method.
(ii) 2's Complement method.
(d) What is the range of signed and unsigned decimal values that can be represented by 8 -bits?
Q. 2. (a) Perform the BCD addition of numbers 286 and 548.
(b) Design a Gray to Binary code converter using NAND gates only.
$\mathrm{F}(\mathrm{W}, \mathrm{X}, \mathrm{Y}, \mathrm{Z})=\square(0,2,5,6,8,10)$
(c) Convert the decimal number 3567 to
(i) Hexadecimal Number
(ii) Octal Number
Q. 3. (a) Show how the following expression can be implemented using NAND gates only. $\mathrm{X}=(\mathrm{A}+\mathrm{B})(\mathrm{C}+\mathrm{D})$
(b) For the following circuit, determine the Boolean function for the output F .
Q. 4. (a) Minimize the four variable logic function.
$\mathrm{f}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})=(\mathrm{A}+\mathrm{B}+\mathrm{C}+\mathrm{D})(\mathrm{A}+\mathrm{C}+\mathrm{D}) .(\mathrm{A}+\mathrm{B}+\mathrm{C}+\mathrm{D})$.
$(B+C) \cdot(B+C) \cdot(A+B) \cdot(B+D)$
(b) Implement the expression using 8:1 multiplexer
$\mathrm{f}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})=\mathrm{m}(0,2,3,6,8,9,11,14)$
Q. 5. (a) What do you understand by race around condition in a J-K flip flop? How is it removed in J-K master Slave flip-flop? Explain the working of masterslave flip-flop in detail by giving its block diagram and truth table.
(b) Design a J-K type synchronous counter to count the following states.
$5,8,2,7,13,0,5$,
Q. 6. (a) Explain the working of an 8-bit serial-in-parallel-out shift register by giving its block diagram. How long will an 8 bit binary number take in this register if the lock frequency is
(i) 1 Mhz
(ii) 5 Mhz .
(b) Explain the working of an OP-AMP based Schmitt Trigger Circuit.
Q. 7. (a) Explain the ladder method of a D/A converter. How does this method overcome the disadvantages of a weighted register method?
(b) Show how to expand $256 \times 4$ RAMs to obtain a memory expansion of $1024 \times 4$.
Q. 8. (a) Give and explain the concept of a tri-state buffer circuit. Write its advantages also
(b) What is a microprocessor? Give the pin diagram of an $8085 \mu$ p and briefly explain the pin architecture.

Give your answer with reference to the system bus architecture and register organization of $8085 \mu \mathrm{p}$.

