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**2008 VISVESVARAYA TECHNOLOGICAL UNIVERSITY**

THIRD SEMESTER B.E. DEGREE EXAMINATION
LOGIC DESIGN

DEC.08/JAN.09 TIME: 3 HRS.
MARKS: 100

**Note:l. Answer any FIVE full questions, choosing at least two questions from each part A & B. 2. Missing data be suitably assumed.**

Part A

1 a.Convert the given boolean function f(x,y,z) = [x + xz(y + z)] into maxterm canonical formula and hence highlight the importance of canonical formula
(05 Marks)

b.Distinguish the prime implicants and essential prime implicants. Determine the same of the
function f(w,x,y,z) = ?m(0,l,4,5,9,ll,13,15) using K-map and hence the minimal sum expression. (05 Marks)

c. Design a combinational logic circuit, which converts BCD code into Excess-3 code and
draw the circuit diagram. (10 Marks)

2 a. Using Quine-Mcluskey method and prime implicant reduction table, obtain the minimal sum expression for the Boolean function f(w,x,y,z) = pie m(l, 4,6,7,8,9,10,11,15).
(12 Marks)

b. Obtain the minimal product of the following Boolean functions using VEM technique:
f(w,x,y,z) = £m(l,5,7,10,ll) + dc(2,3,6,13)
(08 Marks)

3 a. Realize the following functions expressed in maxterm canonical form in two possible ways using 3-8 line and decoder:
(10 Marks)

f1(x2,x1,x0) = ?M(l,2,6,7)
f2(x2,xl,x0) = ?M(l,3,6,7)

b. What are the problems associated with the basic encoder? Explain, how can these problems
be overcome by priority encoder, considering 8 input lines.
(10 Marks)

4 a. Implement the function f(w,x,y,z) = ]Tm(0,l,5,6,7,9,10,15) using a 4 : 1 MUX with w, x as select lines:
(08 Marks)

b. The 1 -bit comparator had 3 outputs corresponding to x > y, x = y and x < y. It is possible to
code these three outputs using two bits S1S2 such as Si, So = 00, 10, 01 for x = y, x > y and
x < y respectively. This implies that only two-output lines occur from each 1-bit

comparator. However at the output of the last 1-bit comparator, an additional network must
be designed to convert the end results back to three outputs. Design such a 1-bit comparator
as well as the output converter network.

(12 Marks)

## Part B

5 a. What is a Flip Flop? Discuss the working principle of SR Flip Flop with its truth table. Also highlight the role of SR Flip Flop in switch debouncer circuit.

(08 Marks)

b. With neat schematic diagram of master slave JK-FF, discuss its operation. Mention the advantages of JK-FF over master-slave SR-flip-flop.

(12 Marks)

6 a. Design a 4-bit universal shift register using positive edge triggered D flip-flops to operate as shown in the table below Q6 (a)

(12 Marks)

Select line Data line selected Register operation
So Si
0 0 I0 HOLD
0 1 I1 Shift RIGHT
1 0 I2 Shift LEFT
1 1 I3 Parallel load
Table Q6 (a)

b. Explain the working principle of a mod-8 binary ripple counter, configured using positive edge triggered T-FF. Also draw the timing diagram.

(08 Marks)

7 a. Distinguish between Moore and Mealy model with necessary block diagrams.

(08 Marks)

b. Give output function, excitation table and state transition diagram by analyzing the sequential circuit shown in figure Q7 (b)

(12 Marks)

Fig. Q7 (b)

8 a. Construct Moore and Mealy state diagram that will detect input sequence 10110, when input pattern is detected, z is asserted high. Give state diagrams for each state,

(10 Marks)

b. Design a cyclic mod 6 synchronous binary counter using JK flip-flop. Give the state diagram, transition table and excitation table.

(10 Marks)