CODE NO: NR 310201 NR

2006 JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY

III B.TECH I SEMESTER SUPPLEMENTARY EXAMINATIONS
COMPUTER ORGANIZATION
(COMMON TO ELECTRICAL & ELECTRONIC ENGINEERING, ELECTRONICS & COMMUNICATION ENGINEERING, ELECTRONICS & INSTRUMENTATION ENGINEERING AND ELECTRONICS & TELEMATICS)

NOVEMBER 2006

TIME - 3 HOUR
MARK – 80

Answer any FIVE Questions
All Questions carry equal marks

1. *(a) Give the general structure of a Von Neumann machine and describe the function of each unit.?*
(b) Describe using flow chart, how an instruction is executed in an IAS computer.

[8+8]

2. *Write about Skip and Subroutine call instructions. Illustrate with an example.* *[16]*

3. *With a neat diagram explain the internal organization of 8085. Clearly explain the functions of various registers in 8085* *[16]*

4. *Consider an accumulator based CPU with the following eight one address instructions. LOAD X, STORE X, ADD X, AND X, JMP X, JMPZ X, CMPL, (Complement Accumulator), and RSHIFT. Give fetch and execute cycle operations and identify the necessary control signals to be generated for the above instructions by a micro programmed control unit . [16]*

5. *(a) Define the following terms:*
i. Hit ratio
ii. Miss ratio

(b) What do you mean by cache coherence problem?

(c) Explain how cache memories can be used in paging technique.

[4+6+6]

6. *Compare and contrast segmentation technique with paging technique.* *[16]*

7. *What is Asynchronous Data Transfer? Explain various methods of asynchronous data transfer with timing diagrams.* *[16]*

8. *(a) Differentiate between programmed I/O and memory mapped I/O.*

(b) Compare interrupt I/O control with DMA I/O control. Why does DMA have priority over CPU when both requests a memory transfer?