CODE NO : NR 310404 N6

2005 JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY

III B.TECH I SEMESTER SUPPLEMENTARY EXAMINATIONS
LINEAR & DIGITAL IC APPLICATIONS

(COMMON TO ELECTRONICS & COMMUNICATION ENGINEERING, ELECTRONICS & INSTRUMENTATION ENGINEERING, ELECTRONICS & CONTROL ENGINEERING, MECHATRONICS AND ELECTRONICS & TELEMATICS)

NOVEMBER 2005

TIME – 3 HOUR
MARK – 80

Answer any FIVE Questions
All Questions carry equal marks

1.(a) What are the three differential amplifier configurations? Compare and con- trast these configurations.

(b) what is a level translator circuit? Why is it used with the cascaded differential amplifier used in OP-AMPS?

(c) Explain the term ''Slew Rate'' and how it affects the frequency response of an an OP-AMP? [5+5+6]

2. (a) Explain the differences between ac and dc amplifiers

(b) What is instrumentation amplifier? What are its features? List any three applications of instrumentation amplifier. [10+6]

3. (a) Derive the frequency of oscillation of a RC phase shift oscillator and explain the operation of the circuit.

(b) Define supply voltage sensitivity. What is meant by poorly regulated power supply? [10+6]

4. Discuss, with relevant circuits and waveforms, the working of Monostable multivibrator using 555 timer. [16]

5. (a) What is the working principle of PLL? Explain.
(b) Give the block diagram of PLL and explain about each block in detail.
(c) Give any one application of PLL. [4+6+6]

6. (a) Explain the operation of a delay equalizer circuit with neat sketches. Derive an expression relating input and output voltages of the equalizer.

(b) For the all pass filter, determine the phase shift between input and output at f=2 kHz. To obtain a positive phase shift. What modifications are necessary in the circuit? [6+10]

7. (a) What is meant by Tri-state logic ? Draw the circuit of Tri-state TTL logic and explain its functions.

(b) Draw the circuit of ECL logic OR/NOR gate and explain its functions. [10+6]

8. (a) i. CompCode No: NR310404 NR ii. Why successive approximation D/A converter is preferable than parallel comparator A/D converter. Explain. [10+6]

(b) Draw the schematic block diagram of Dual-slope A/D converter and explain its operation. Derive expression for its output voltage Vo.are weighted resistor D/A converter and R-2R D/A converter.